

# MS-7A32 Ver:11

## CPU:

AMD AM4

## System Chipset:

Promontory X370/B350  
(Performance gaming)

## Main Memory:

DDR IV \* 4 MAX:64 GB

## VRM

RT8894A 4+2

## On Board Chipset:

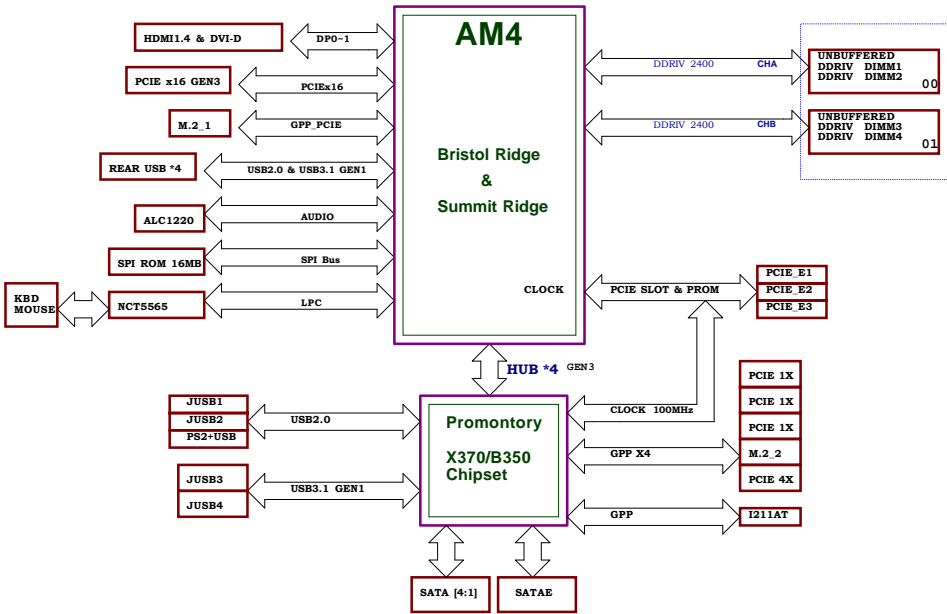
LPC Super I/O --NCT6795D

LAN I211AT

Azalia CODEC - Realtek ALC1220

ASM2142 USB3.1 Gen2

## FUSION BLOCK DIAGRAM



## Expansion Slots:

From CPU  
PCI Express X16 Slot \* 1  
PCI Express X8 Slot \* 1

From FCH  
PCI Express X1 Slot \* 1  
PCI Express X1 Slot \* 1  
PCI Express X1 Slot \* 1  
PCI Express X4 Slot \* 1

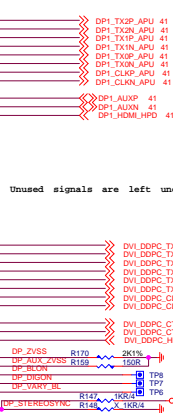
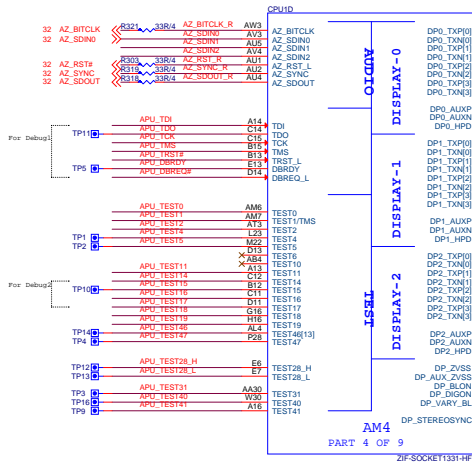
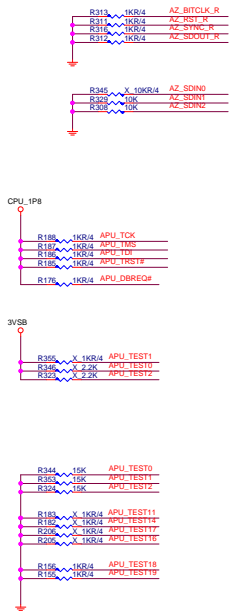
## OCP IC:

UP6273

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27 USB Front Side	
28 SATA Connector	
29 DVI Connector	
30 DP to VGA ITE6516	
31 ACPI uPI-5VDIMM&3VSB	
32 PM-NB681-1.05V/GS7133-2.5V	
33 DDR PWR VPP25/VTT-MP2143	
34 DDR Power-RT8231AGQW	
35 CPU Power 1P8V-MP2147	







For HDMI

For DVI

Unused signals are left unconnected.

Not supported on AMD Family 17h/Models 00h-0Fh

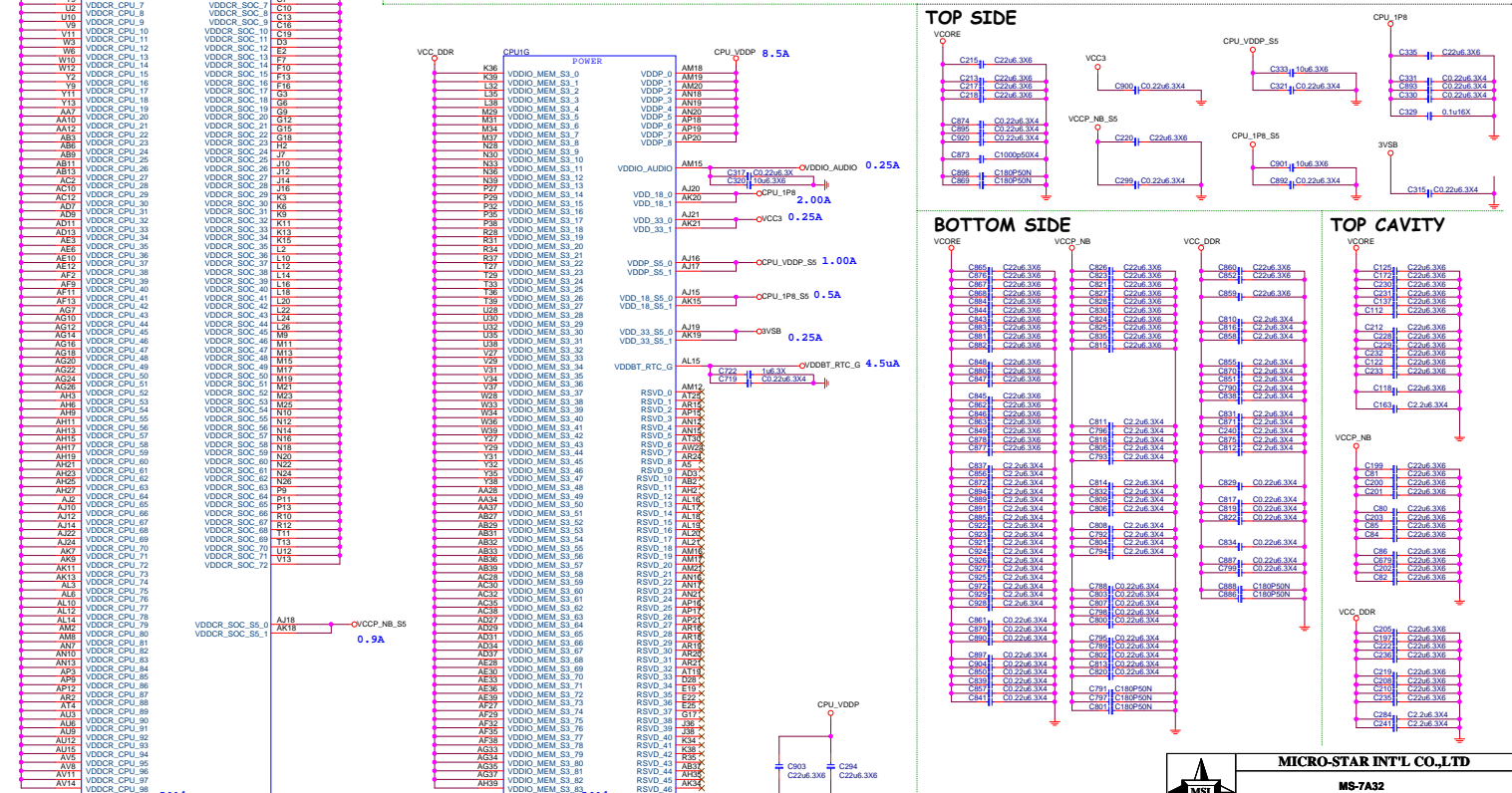
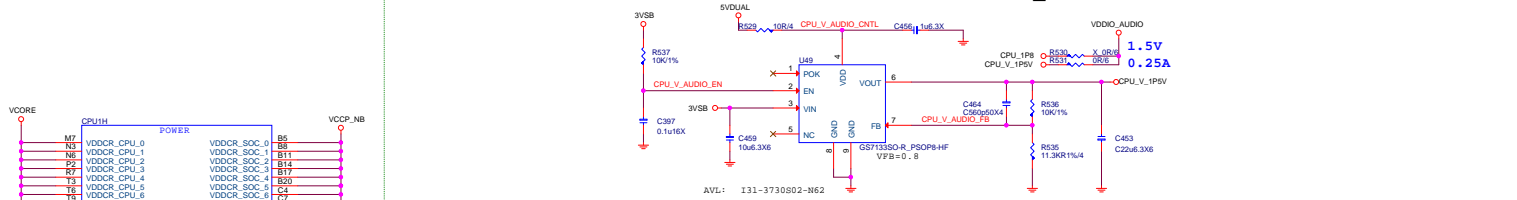
Not support Type2







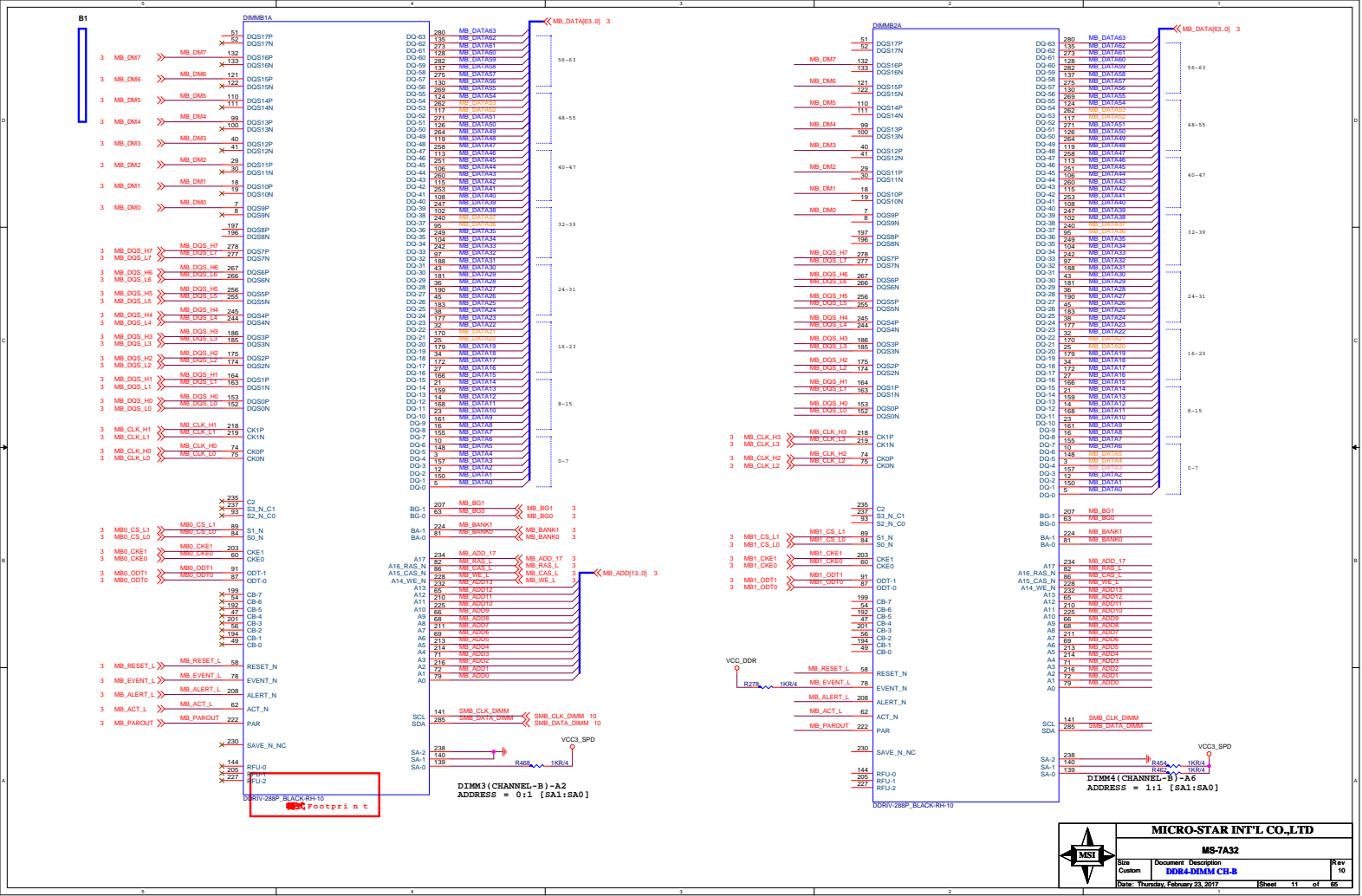
### VDDIO\_AUDIO Circuit





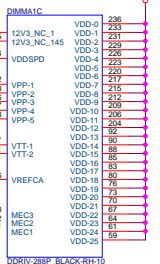




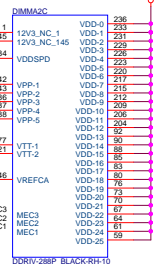




DIMM SLOT PN BY SPEC



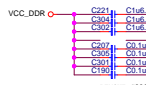
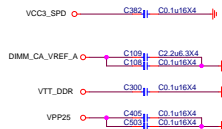
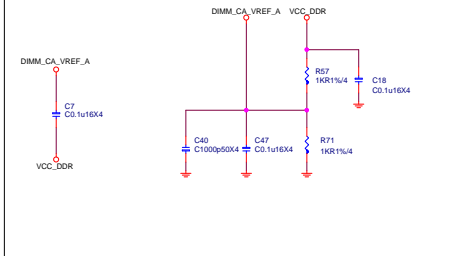
DORIV-28BP\_BLACK-RH10



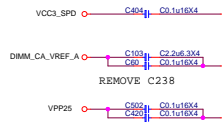
DORIV-28BP\_BLACK-RH10

## DDR VREF

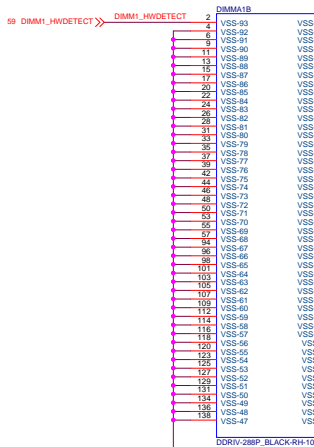
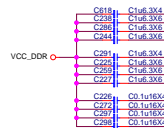
(place resistors close to DIMMs)



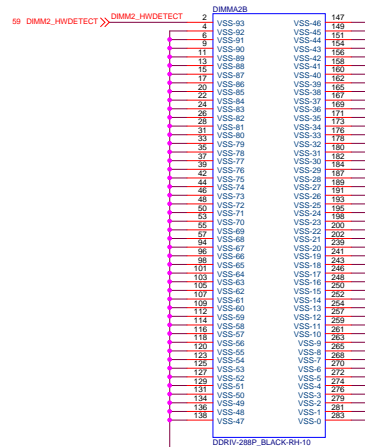
REMOVE C286



REMOVE C238



DORIV-28BP\_BLACK-RH10



DORIV-28BP\_BLACK-RH10



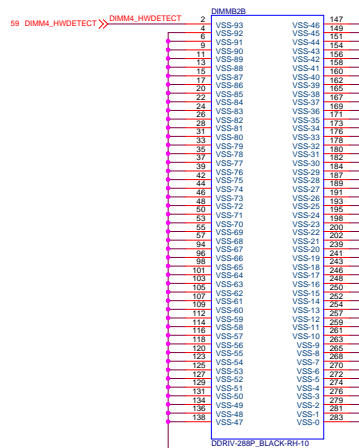
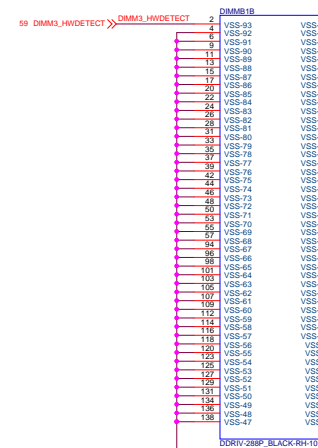
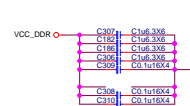
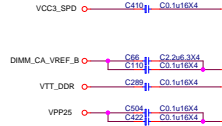
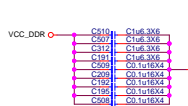
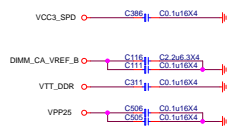
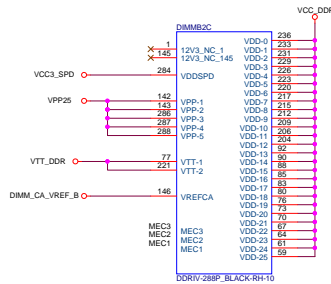
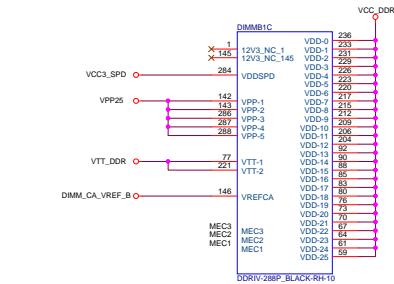
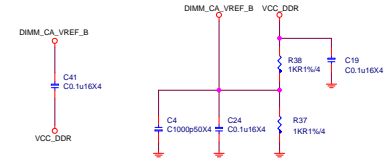
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# DDR VREF

(place resistors close to DIMMs)

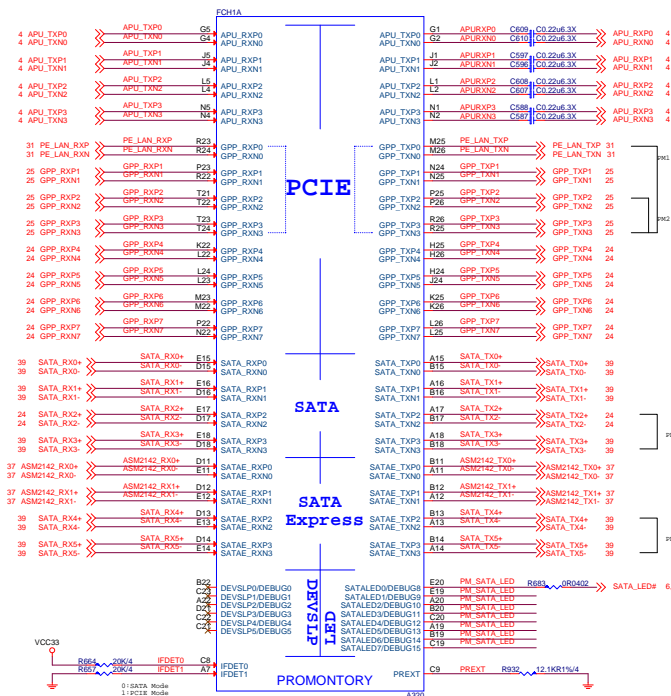


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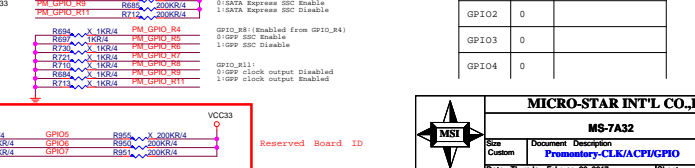
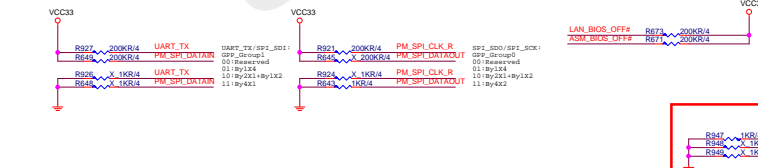
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Size	Document Description
Custom	<b>Promontory-PCIE/SATA/SATAE</b>

Rev	10
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**BOM OPTION**

VCC3

RE29 X 10K R4 GP102 RE30 10K  
R64 X 10K R4 GP103 R64 10K  
R65 X 10K R4 GP104 R65 10K

FULL

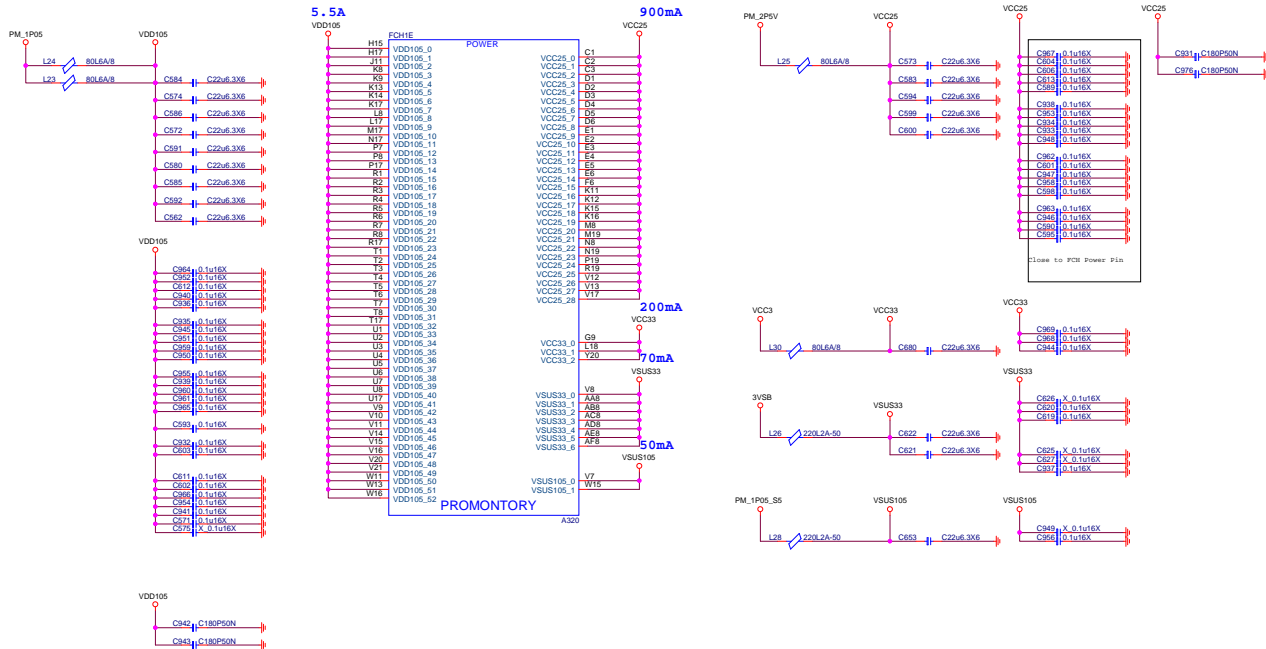
GP102	0
GP103	0
GP104	0

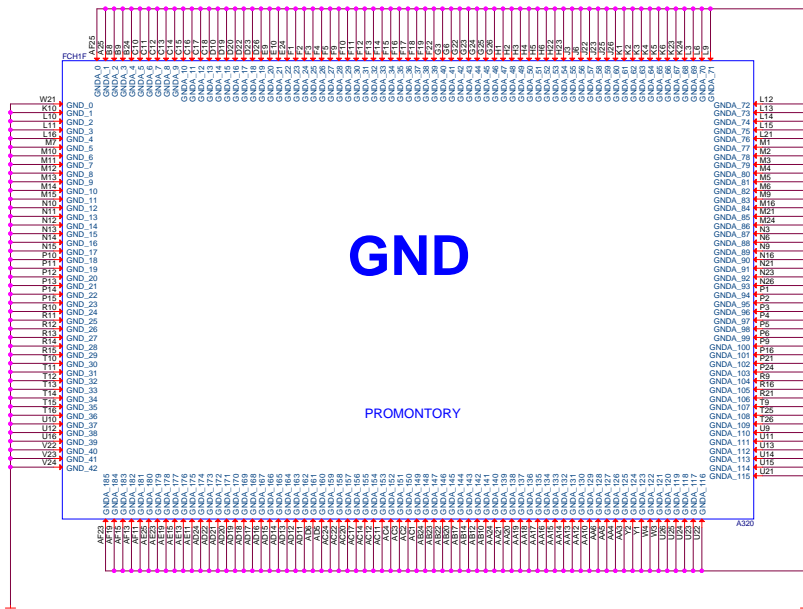
**MICRO-STAR INT'L CO.,LTD**

**MS-7A32**

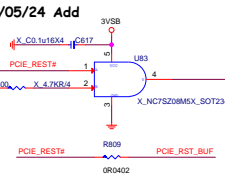
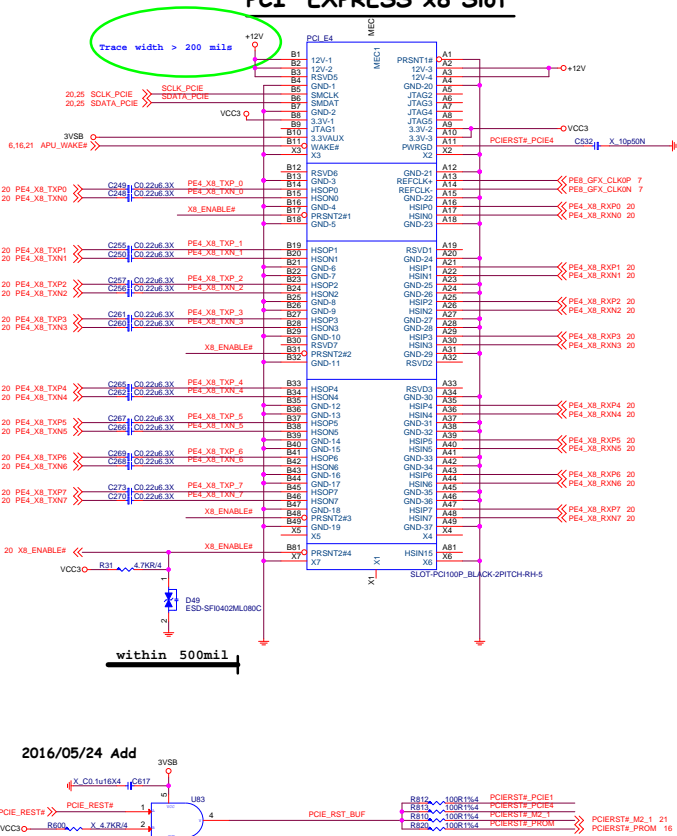
Size	Document Description	Rev
Custom	Promemory-CLK/ACPI/GPIO	10



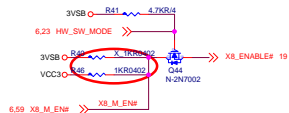
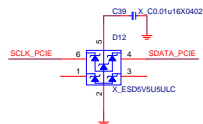
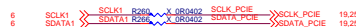




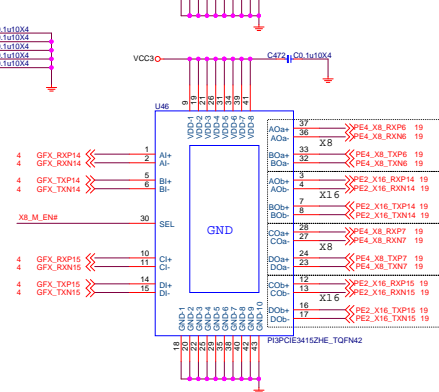
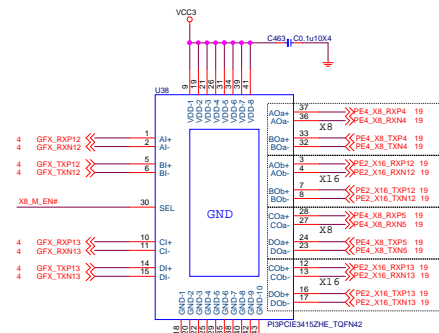
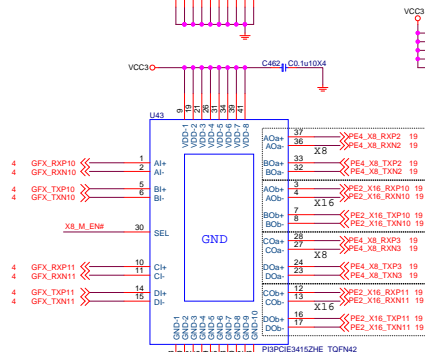
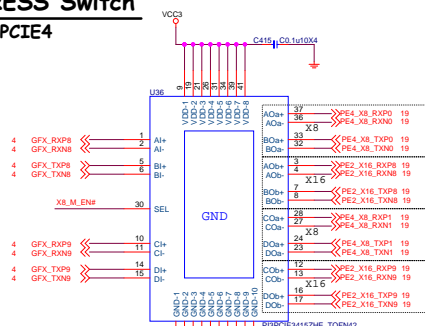
**PCI EXPRESS x8 Slot**



### PCIE Lanes control circuit



	PCIE_CNTL	X8_M_EN#
Auto	1	1
Manual x16	0	1
Manual x8, x8	0	0



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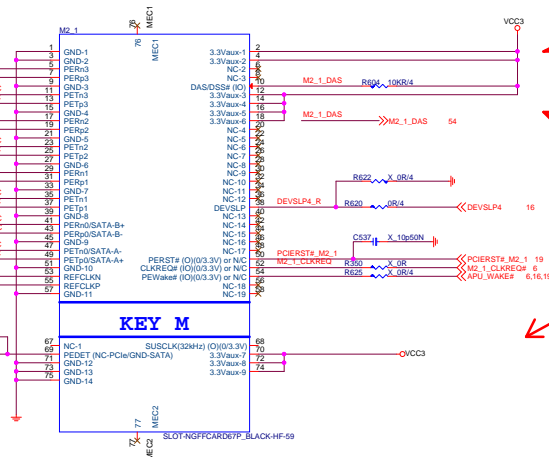
## M.2 Connector

Not supported PCIe on AMD TYPE0 CPU

4 APU\_GPP\_RXN3 APU\_GPP\_RXN3  
4 APU\_GPP\_RXP3 APU\_GPP\_RXP3  
4 APU\_GPP\_TXN3 APU\_GPP\_TXN3  
4 APU\_GPP\_TXP3 APU\_GPP\_TXP3  
22 M2\_RXN2 M2\_RXN2  
22 M2\_RXP2 M2\_RXP2  
22 M2\_TXN2 M2\_TXN2  
22 M2\_TXP2 M2\_TXP2  
4 APU\_GPP\_RXN1 APU\_GPP\_RXN1  
4 APU\_GPP\_RXP1 APU\_GPP\_RXP1  
4 APU\_GPP\_TXN1 APU\_GPP\_TXN1  
4 APU\_GPP\_TXP1 APU\_GPP\_TXP1  
22 M2\_RXP0 M2\_RXP0  
22 M2\_RXN0 M2\_RXN0  
22 M2\_TXN0 M2\_TXN0  
22 M2\_TXP0 M2\_TXP0

PIN 69  
Low SATA  
NC PCIe

VCC0 R620 1K  
6.22 M2\_1\_DET



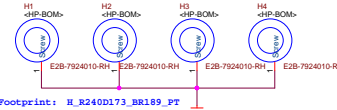
2016.05.31 Update M.2 PartNumber & Footprint  
ON1-7A58001-L06  
SLOT\_NGPPCARD67\_31

VCC3 2.5A

Close to PIN2, 4

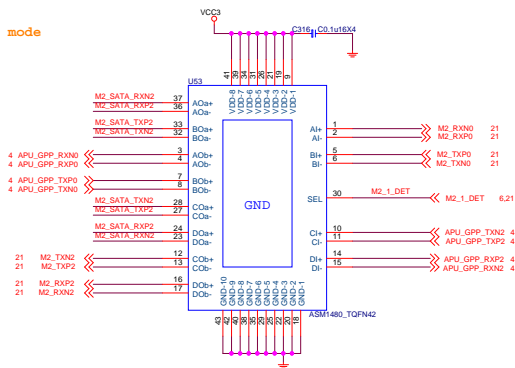
Close to PIN12, 14, 16, 18

Close to PIN70, 72, 74



Footprint: H\_R240D173\_BR189\_PT

Select M2 PCIe or SATA mode



M2\_1\_SW:  
0:SATA  
1:PCIe

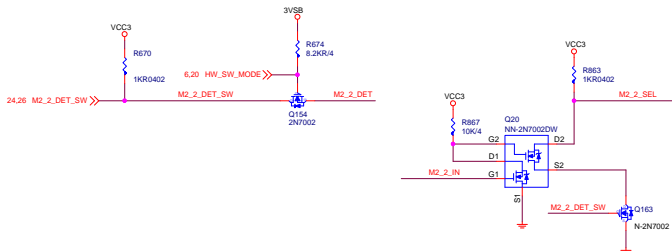
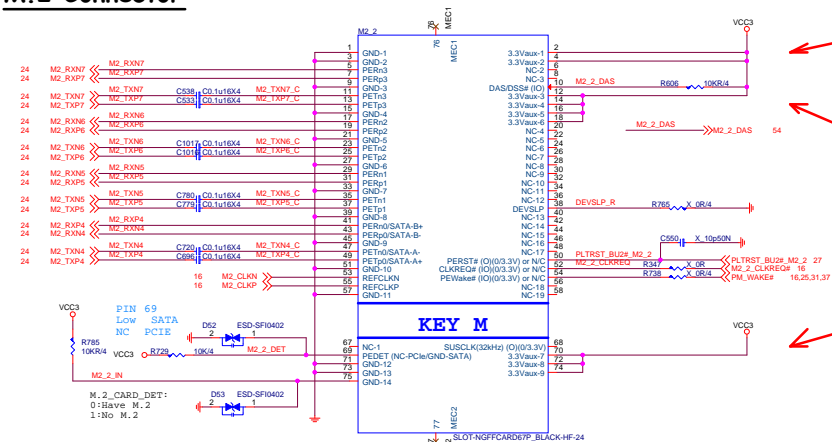


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Custom	M2_1 Switch	10
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## M.2 Connector

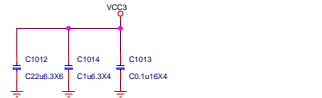


M2	SATA	PCIEX4	M2_2_DET_SW	M2_2_DET_IN	M2_2_DET_SEL
M2 NOT IN	NO	YES	YES	1	1
M2 IN SATA	SATA	NO	YES	0	0
M2 IN PCIE	PCIE	YES	NO	1	0

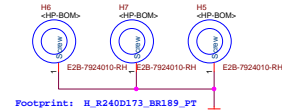
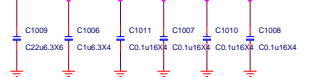
VCC3 2.5A

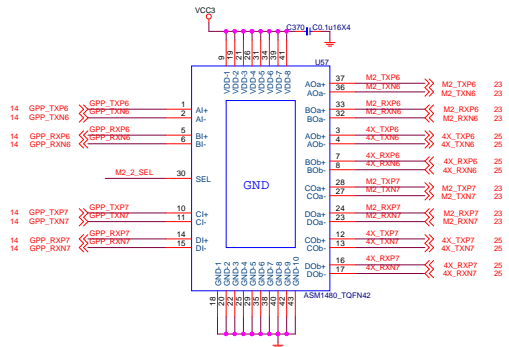
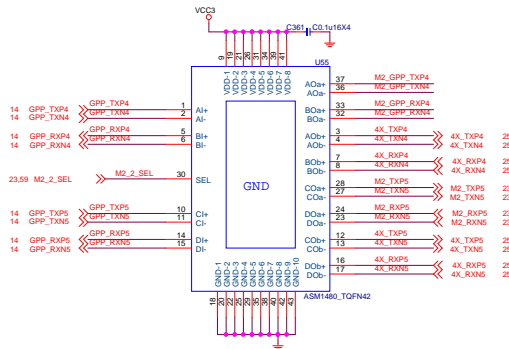
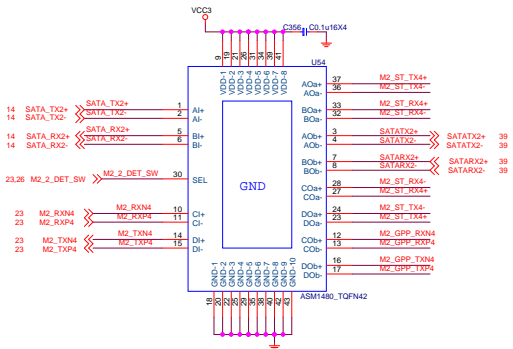


Close to PIN12, 14, 16, 18



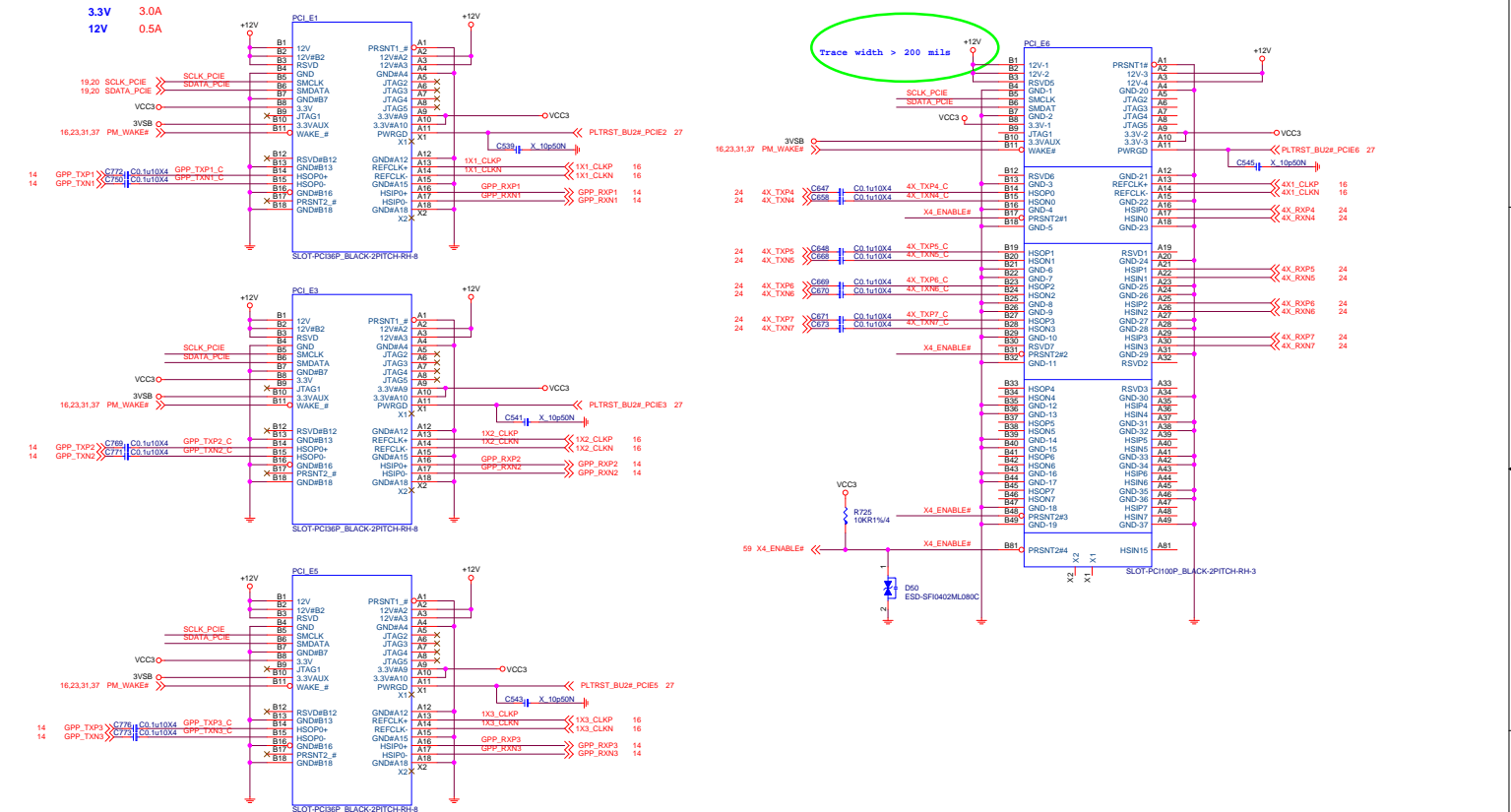
Close to PIN70, 72, 74





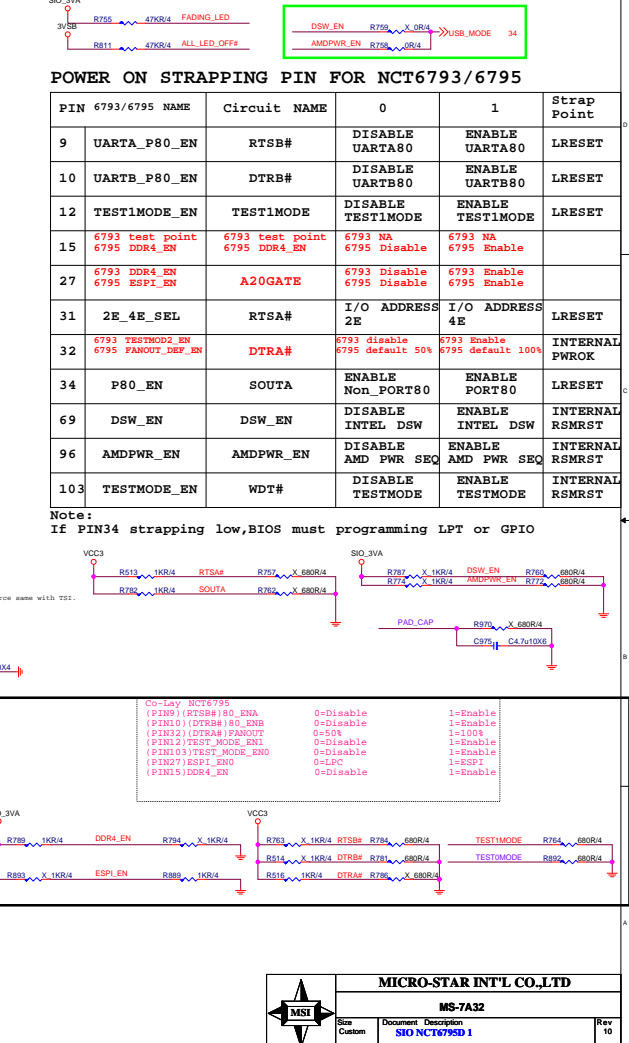
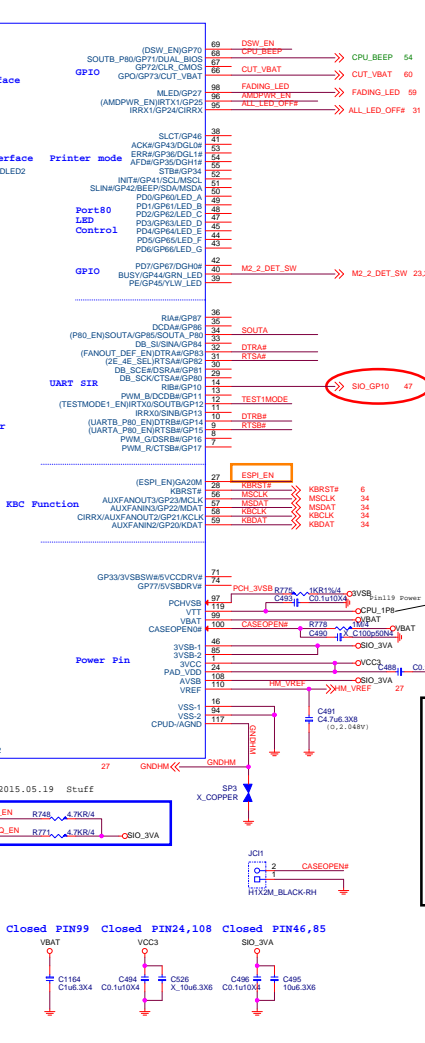
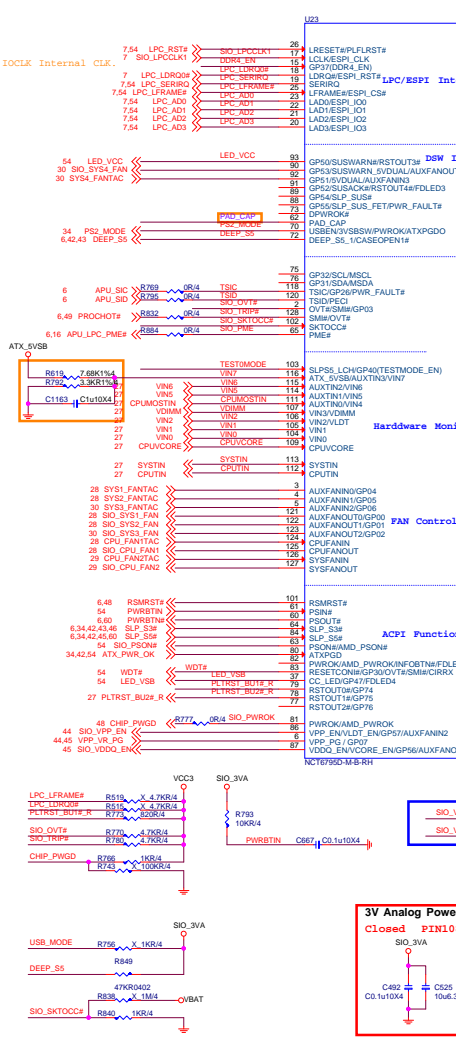


PCIE1X1 12V 0.5A  
3.3V weak 375mA



PCI Express X1 slot	
+12V	- 1 A
+3.3Vaux (wake)	- 750mA
+3.3Vaux (no wake)	- 40mA
+3.3V	- 6.0A

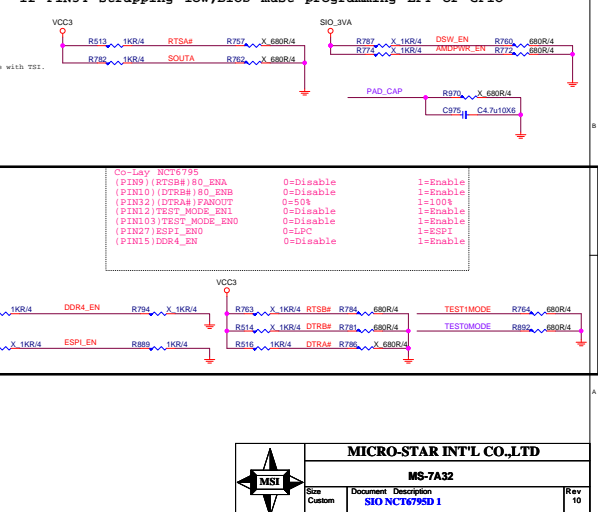
MICRO-STAR INT'L CO.,LTD	
MS-7A32	
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Custom	PCIE 1X 4L
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POWER ON STRAPPING PIN FOR NCT6793/6795

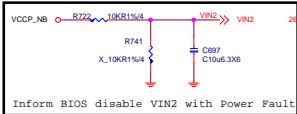
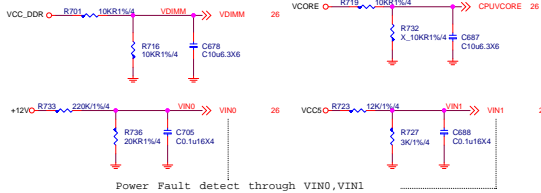
PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TESTMODE_EN	TESTMODE	DISABLE TESTMODE	ENABLE TESTMODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN	A2OGATE	6793 Disable 6795 Enable	6793 Enable 6795 Disable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMODE2 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note: If PIN34 strapping low, BIOS must programming LPT or GPIO



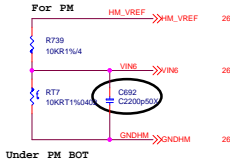
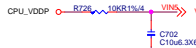
HW Monitor - Voltage

SIO IM Voltage over 2.048V will not detect

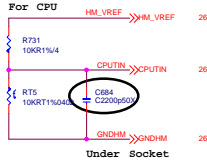


Inform BIOS disable VIN2 with Power Fault

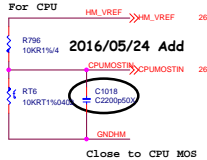
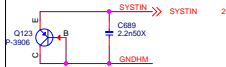
2016/05/24 Remove VIN4



TEMP SENSOR

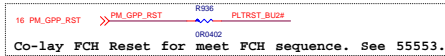
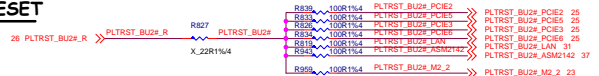


For System



2016/05/24 Add

RESET



From SIO

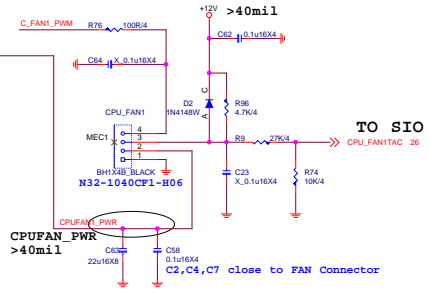


GPIO Control

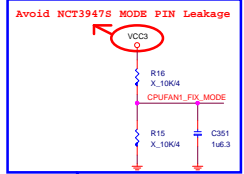
	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

P/N:122-3947S12-N06



TO SIO



Resever For FIX DC or PWM MODE USE By PM SPEC

From SIO

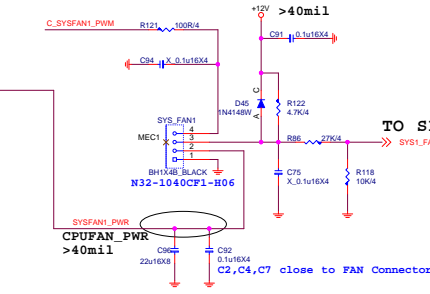


GPIO Control

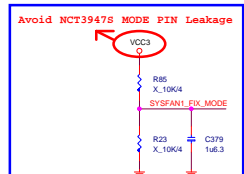
	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

P/N:122-3947S12-N06

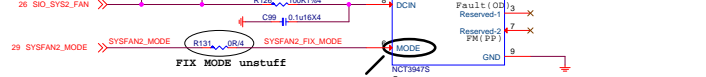


TO SIO



Resever For FIX DC or PWM MODE USE By PM SPEC

From SIO

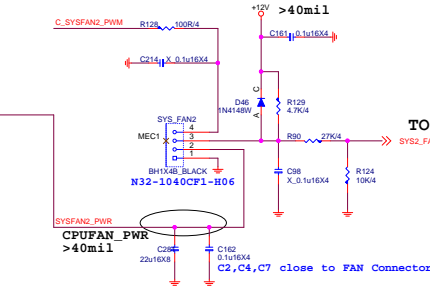


GPIO Control

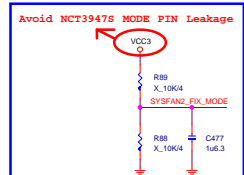
	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

P/N:122-3947S12-N06



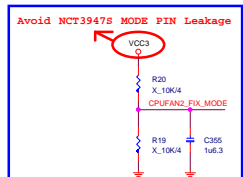
TO SIO



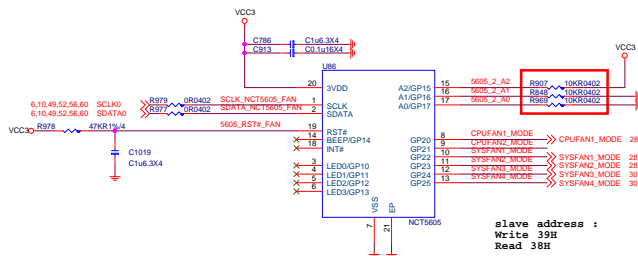
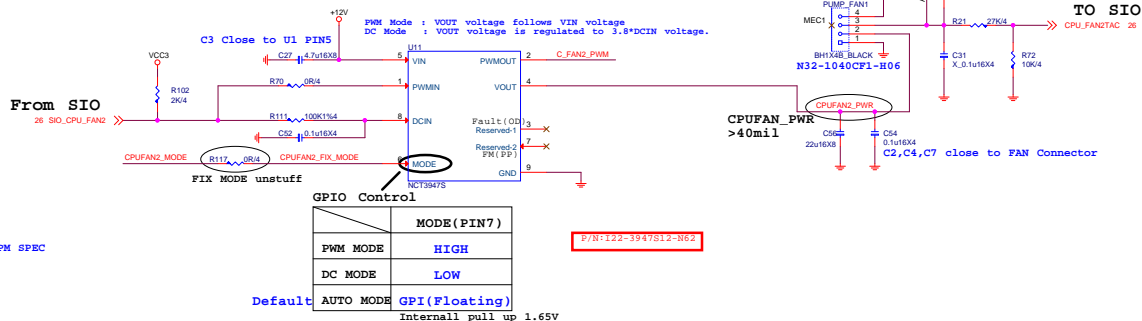
Resever For FIX DC or PWM MODE USE By PM SPEC

# TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

## 2.GPIO 模式 切换 PW M/DC M O D E



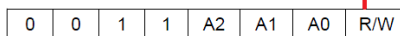
Reasever For FIX DC or PWM MODE USE By PM SPEC



## 1. GENERAL DESCRIPTION

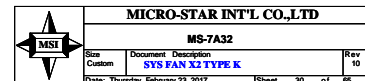
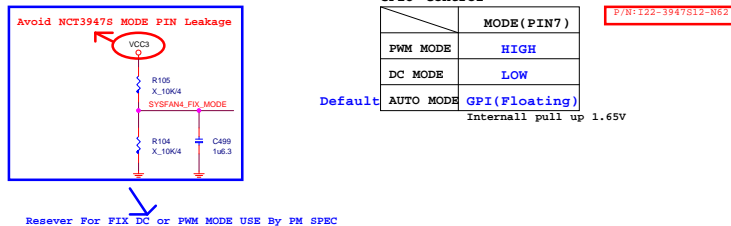
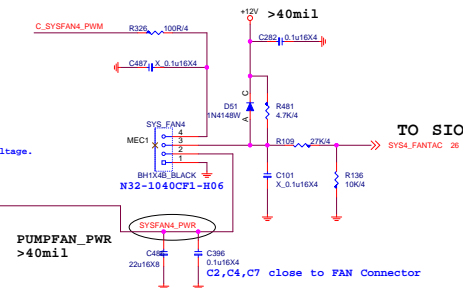
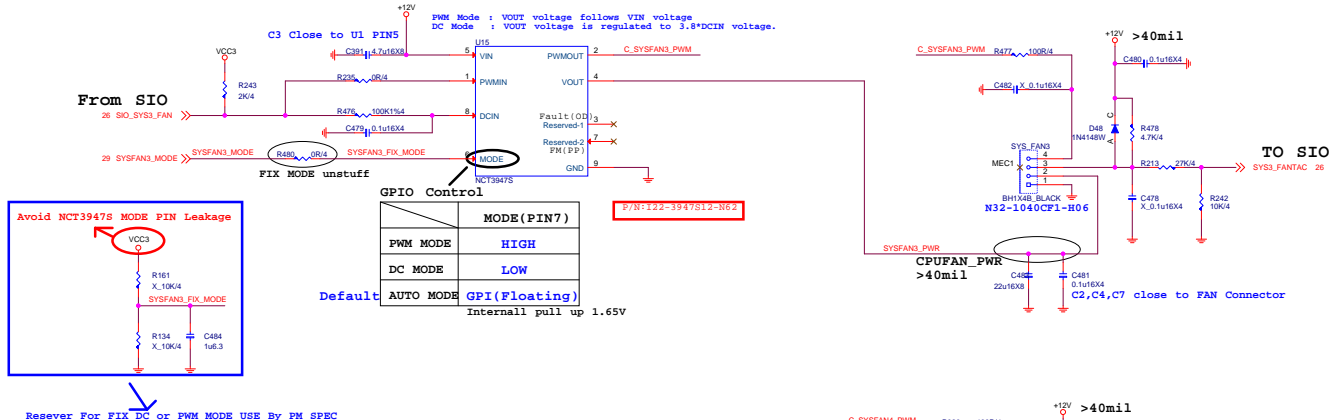
The NCT5605Y is a general purpose input/output IC with SMBus™ which provides 14 GPI/O pins. It also can provide SMBus™ address setting pins to set the address during power-on reset or from external reset.

NCT5605Y SMBus™ Address is:

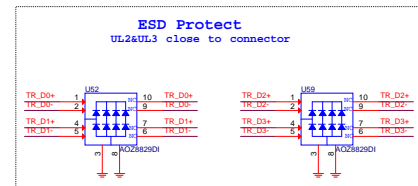
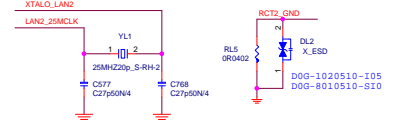
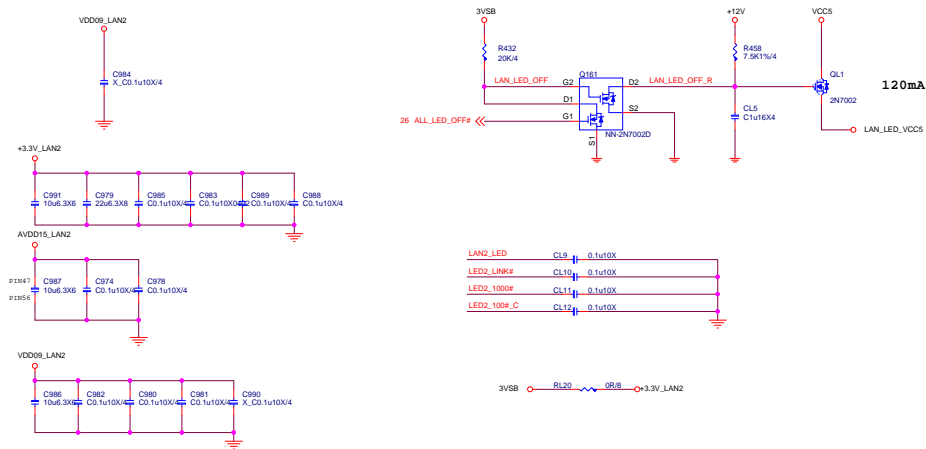
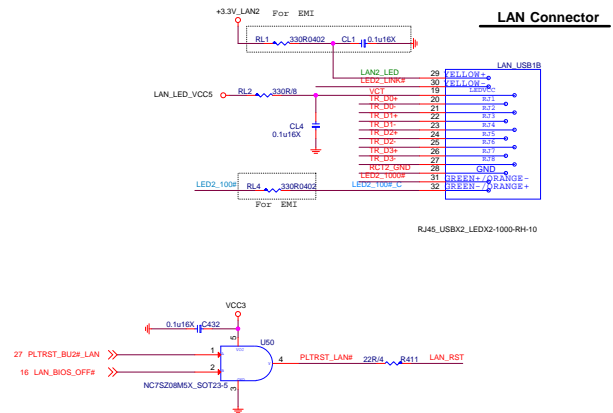
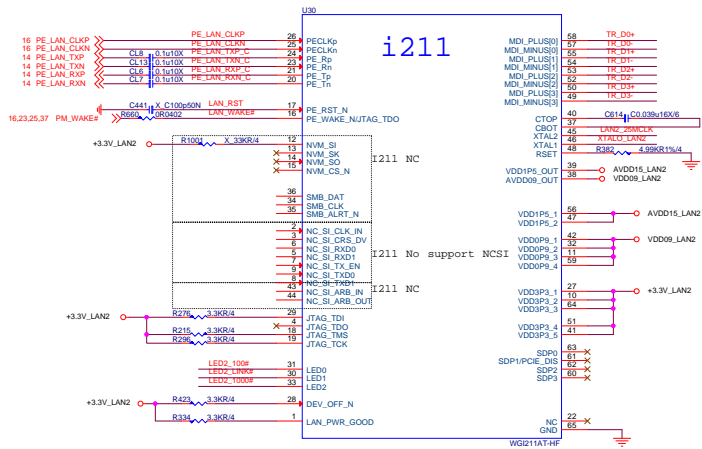


TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

## 2. GPIO 硬件事件 切換 PW M/DC M O D E



**LAN2-- I211AT**

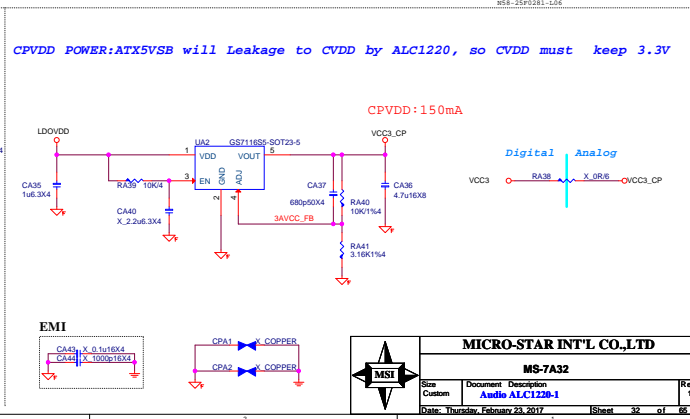
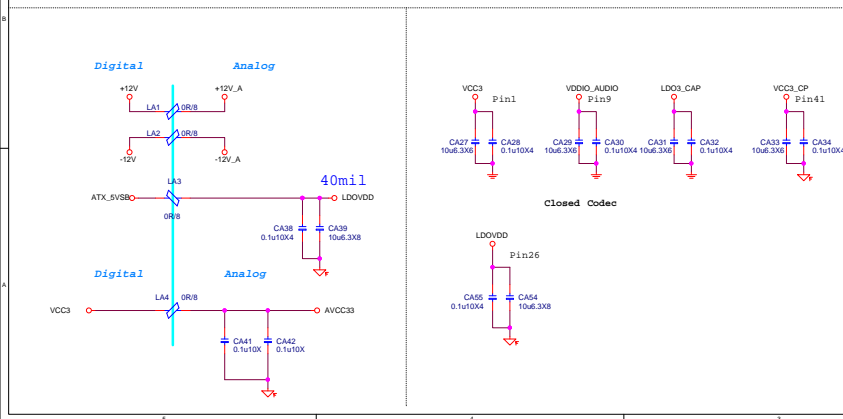
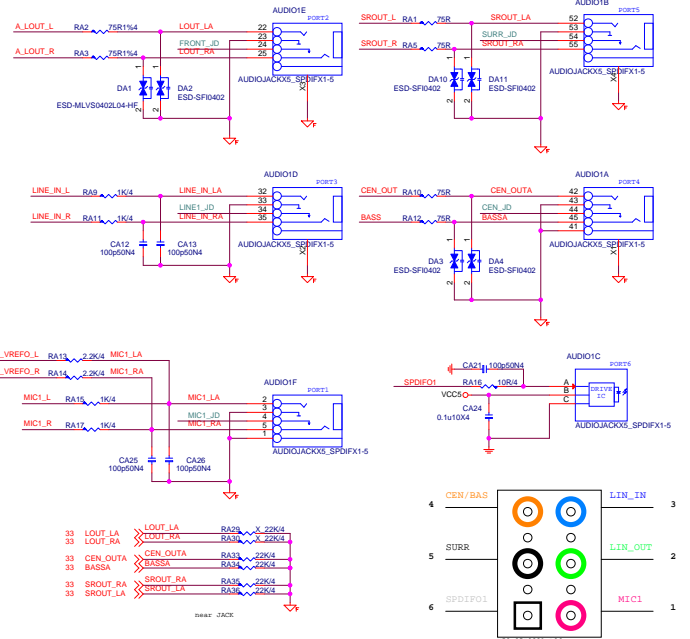
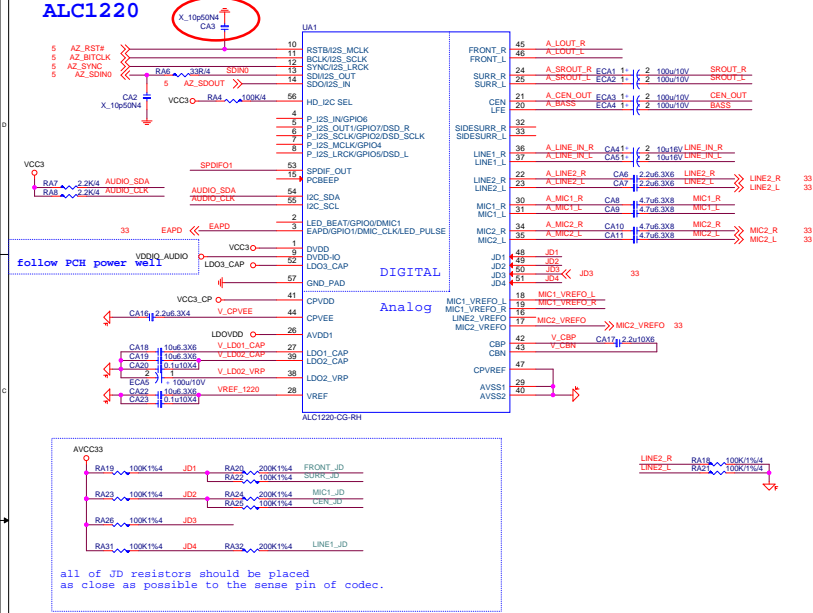


**MICRO-STAR INT'L CO.,LTD**

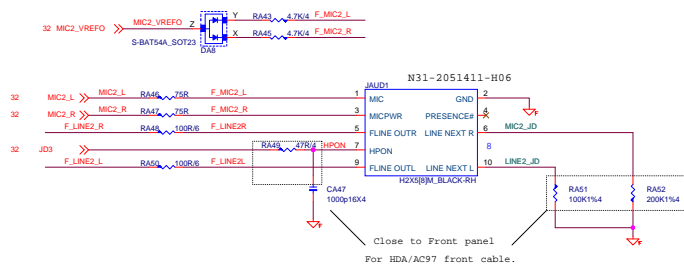
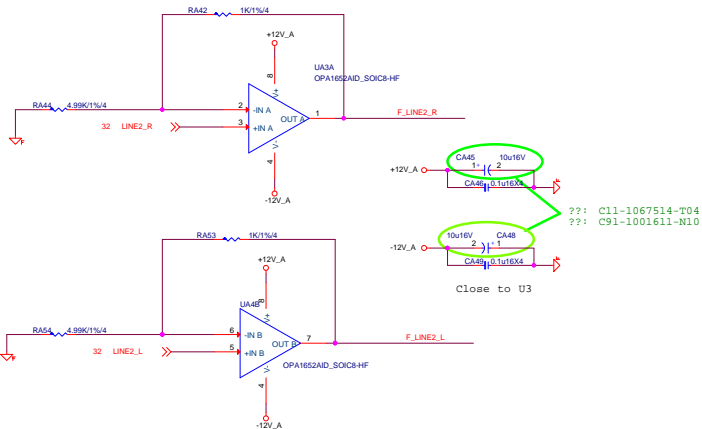
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Size Custom	Document Description <b>LAN-1211AT</b>	Rev 10
Date: Thursday, February 23, 2017		Sheet 31 of 65

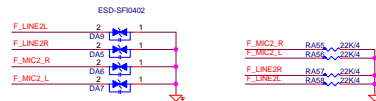
## ALC1220



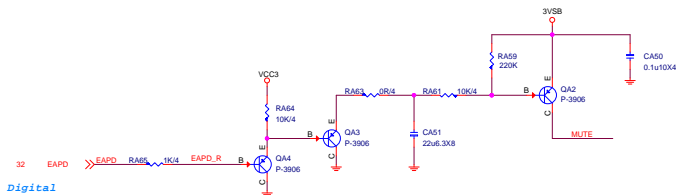




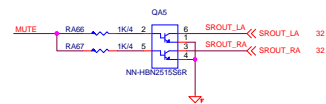
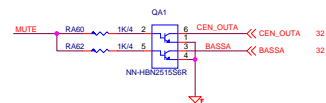
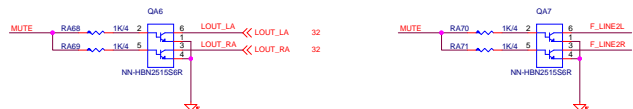
ESD protect  
DQG-2950500-S10  
DQG-2710510-105



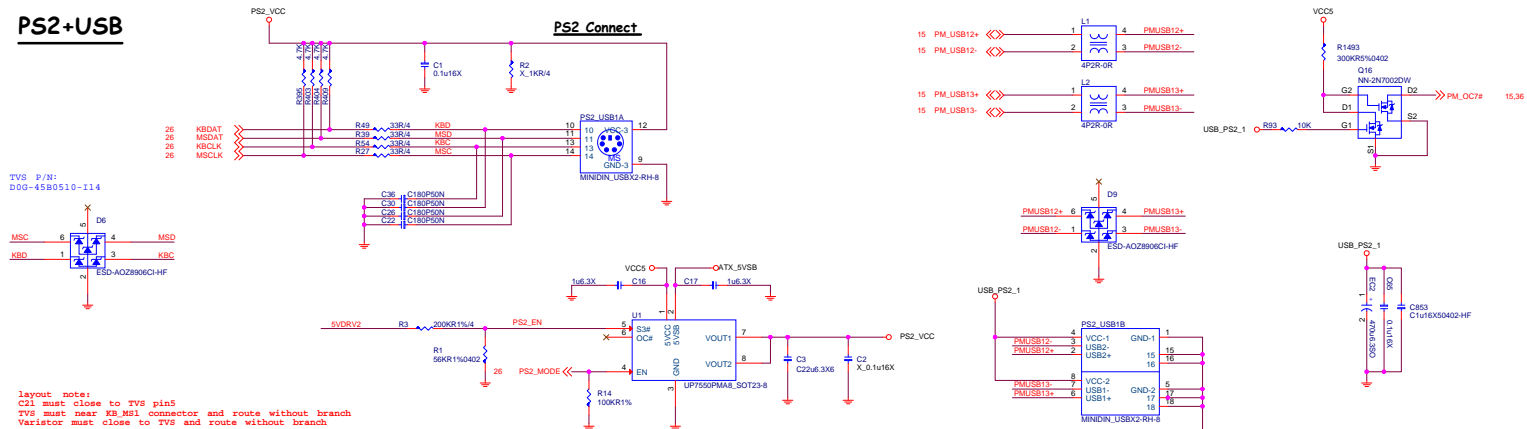
## Rear Line OUT De-POP circuit (De-pop circuit for Rear Line out & Front Headphone out)



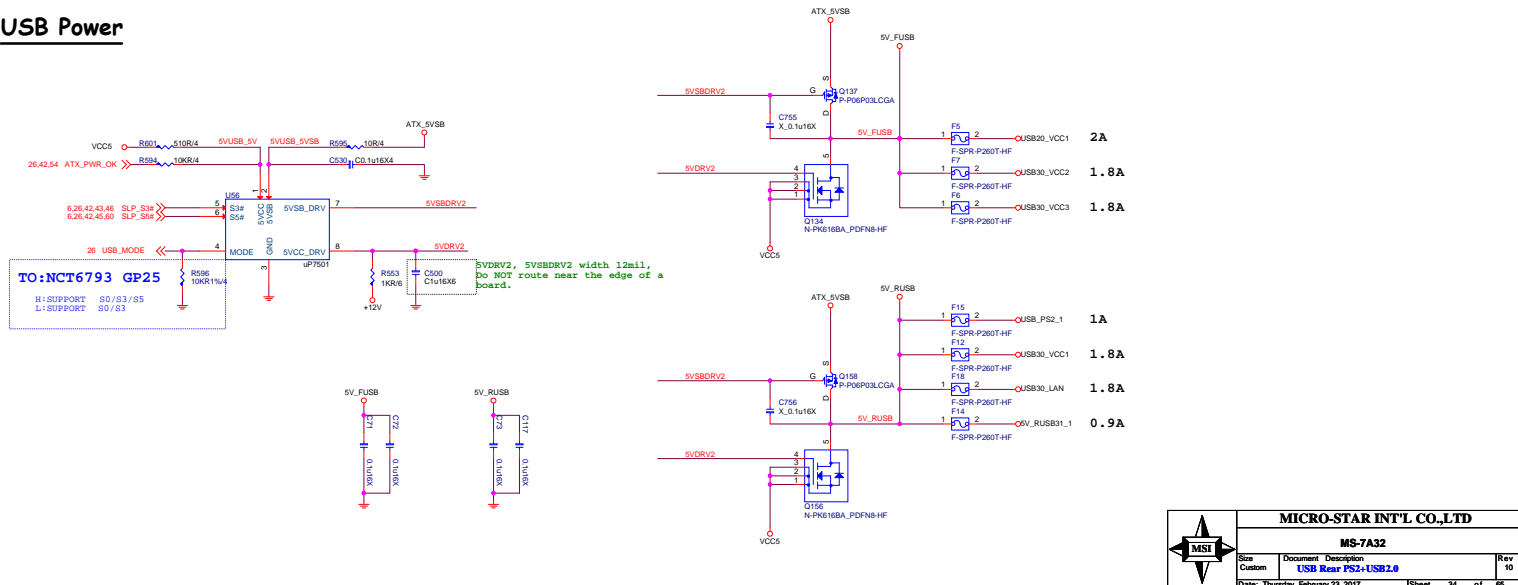
Analog



## PS2+USB

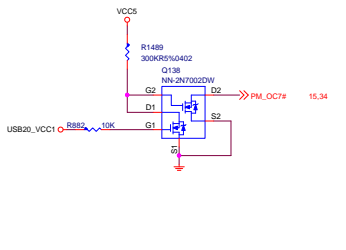
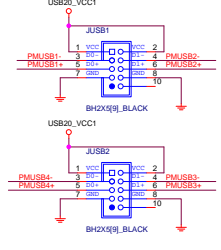
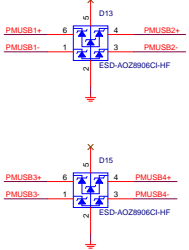
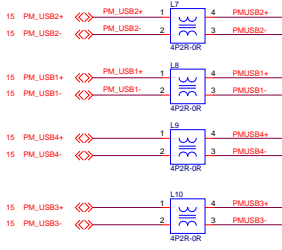


## USB Power

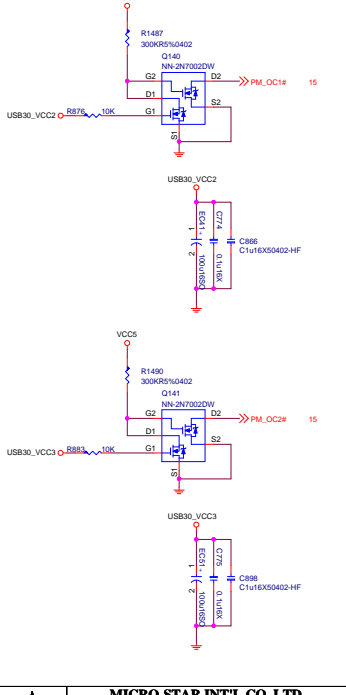
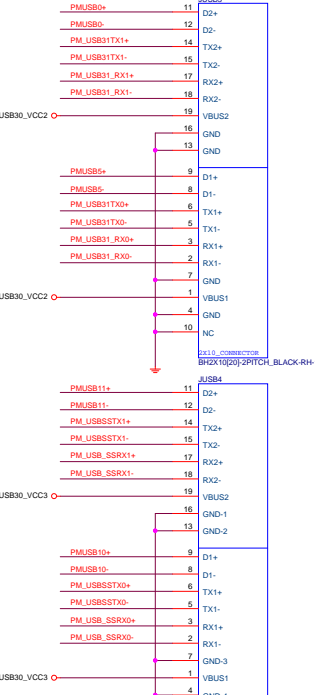
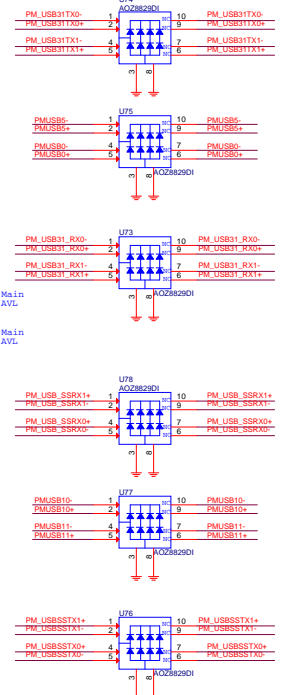
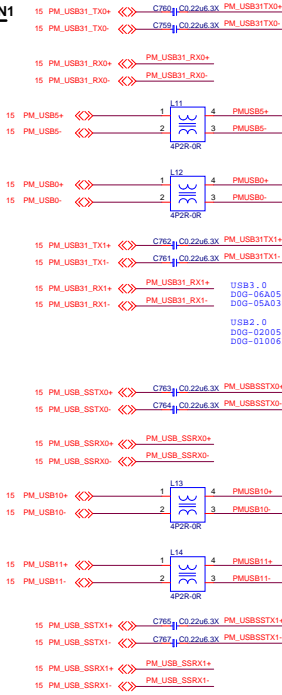




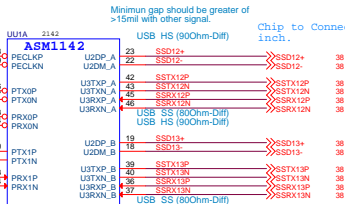
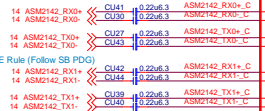
Front USB2.0



Front USB3.1 GEN1



CLK Rule (Follow SB PDG)



Layout Guide:

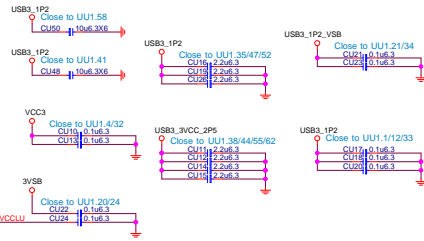
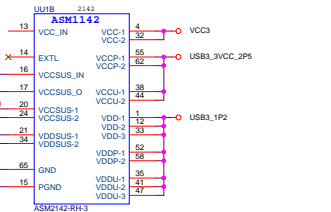
- 1.) USB3.1 to Connector Total Length < 1.5"
- 2.) VIA hole < 2

X0/X1 (95um-Diff Spacing 30mil)  
UREXT1PEUREXT1(W/S) 10/7  
OC1A,OC1B,PPRONA,PPRONB(S) 5/8

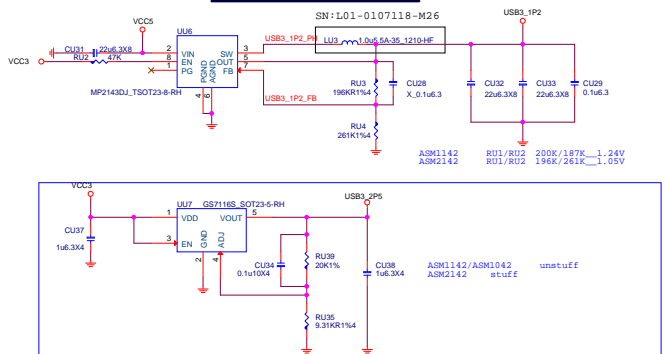


Power Consumption

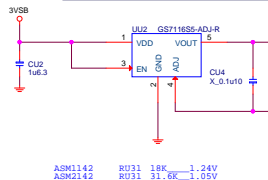
	3.3V	1.2V(1.05V)	3.3VUS	1.05VUS(S1,2VSUS)	2.5V	Total Power
ASM1142	245mA	63mA	1mA	1mA	NA	1573.8(mW)
ASM2142	300mA	800mA	100mA	50mA	300mA	TDP



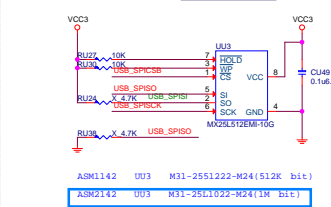
## ASM1142 1.2 VCC Power



## ASM1142 1.2 VSB Power

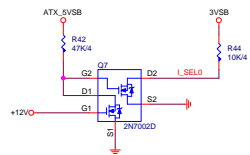


## EEPROM



MICRO-STAR INT'L CO.,LTD			
MS-7A32			
Rev	Document Description	Rev	Rev
1	ASM1142 USB3.1	1	1
Date: Thursday, February 23, 2017	1	1	1

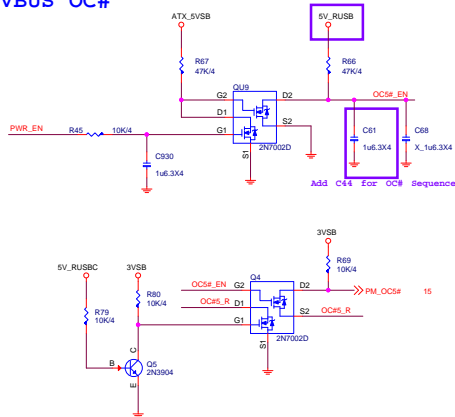
## Current Mode



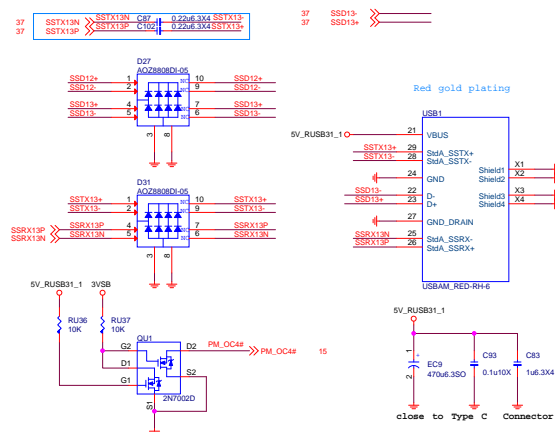
I_SELO - I_SEL1
X 0 Default for 900mA
U 1 1.5A @5V
I 1 3A @5V

1.5A under S3 mode  
3A under S0 mode

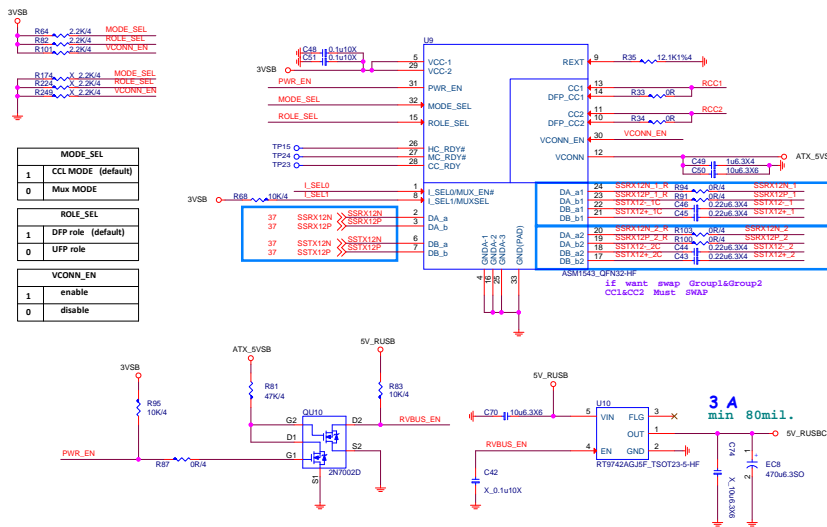
## VBUS OC#



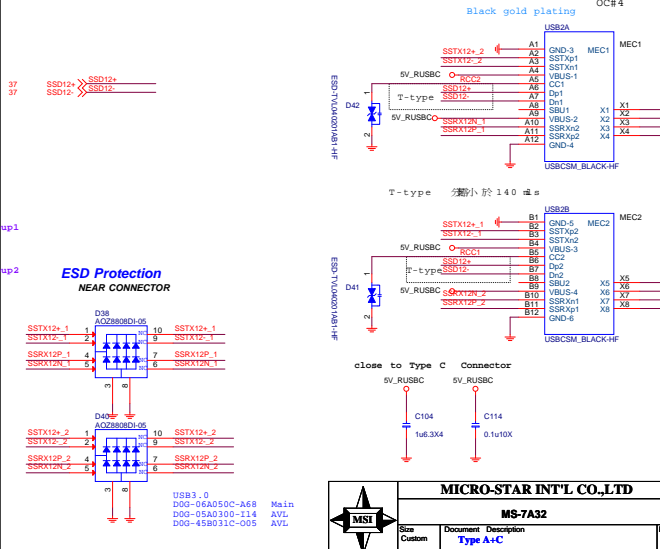
## TYPE-A



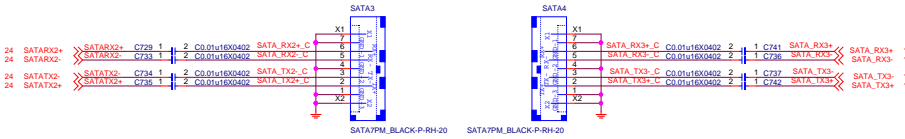
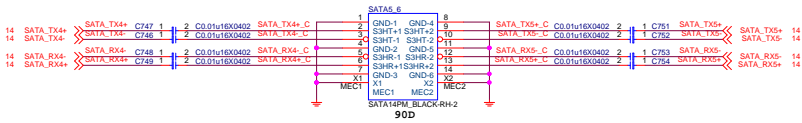
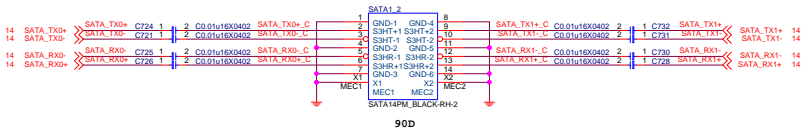
## USB Type-C MUX with Configuration Channel (CC)



## TYPE-C



SATA Connector

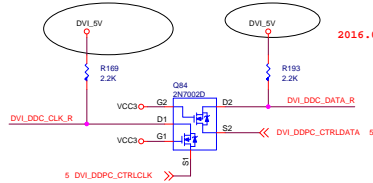


# DVI level shifter

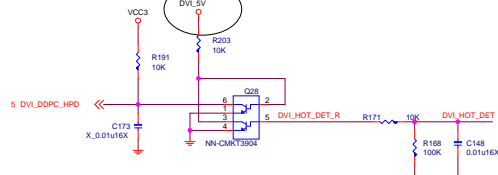
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



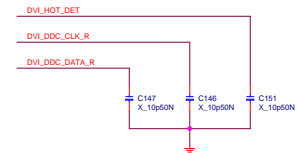
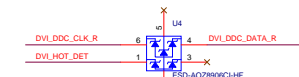
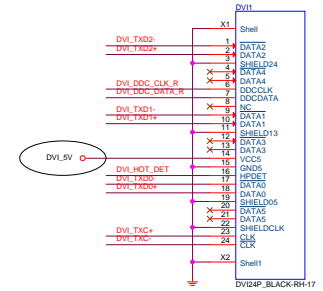
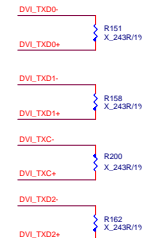
2016.01.11 Dual MOS change to single MOS, reduce CM noise by EMI Suggestion



HPD



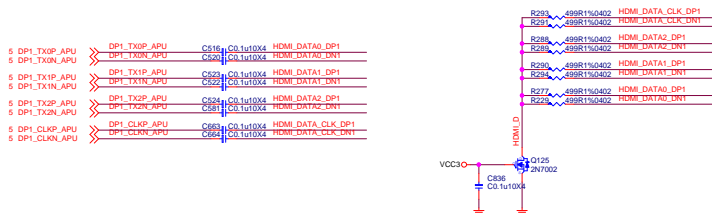
For EMI



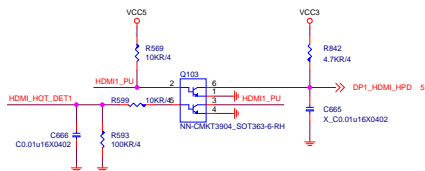


# HDMI CONNECTOR

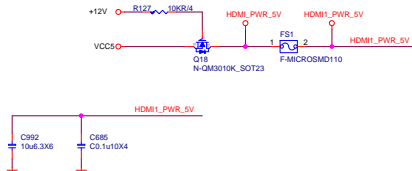
For HDMI 1.4



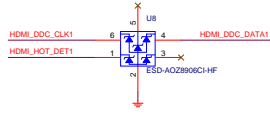
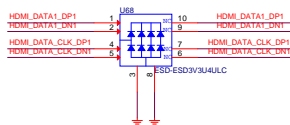
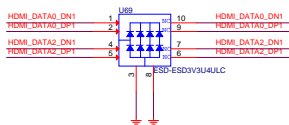
## HPD Circuit



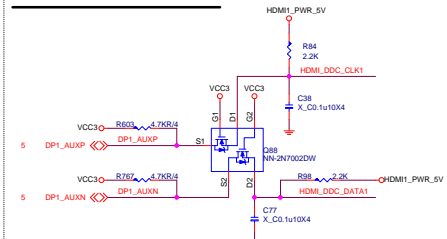
## Connector Power



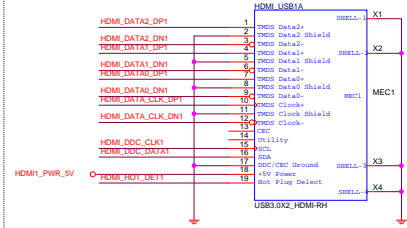
## For EMI



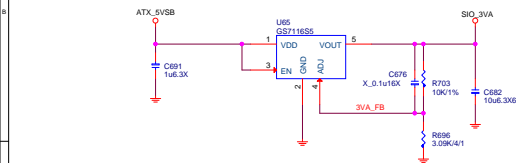
# AUX Level Shifter



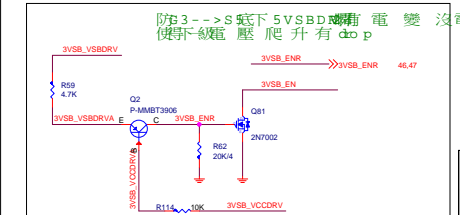
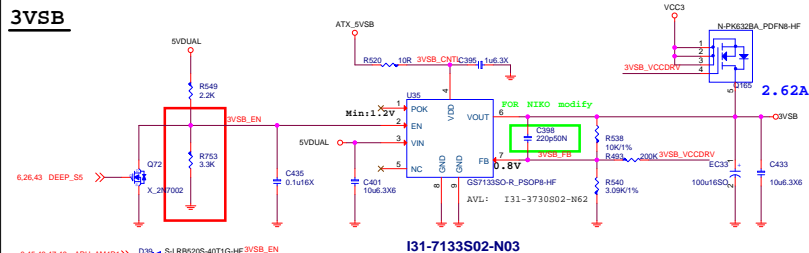
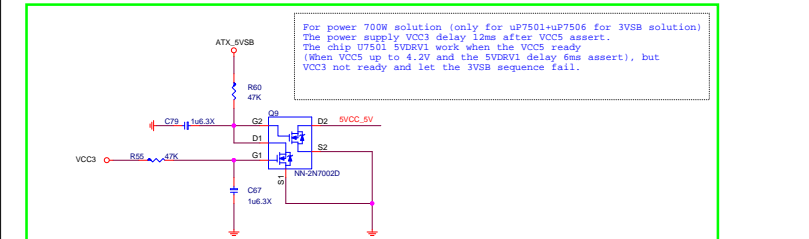
## Connector



**SIO\_3VA**

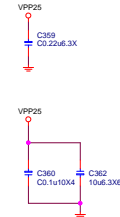
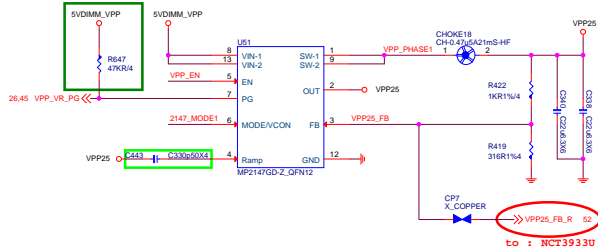


## 3VSB

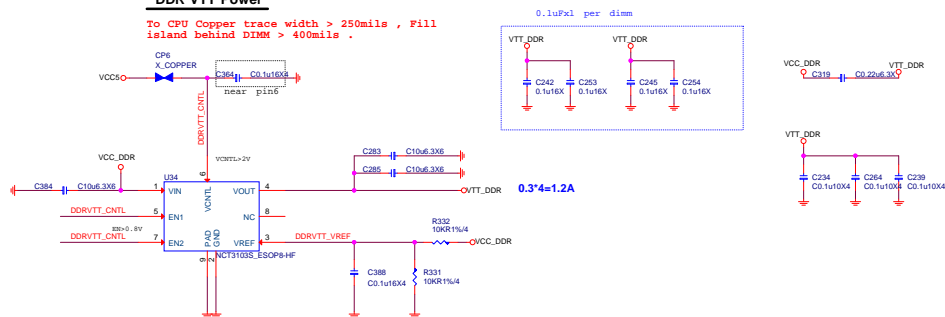


Size Custom	Document Description <b>ACPI wPI-5VDIMM&amp;3VSB</b>	Rev 10
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$$0.7776 \mu H \ll 1.1664 \mu H$$
[illegible][illegible]



To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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DDR4\_1.2V 15.5A+9.5A+1.2A=26.2A

15.5A FOR CPU

9.5A FOR 2DIMM

1.2A FOR DDR VTT

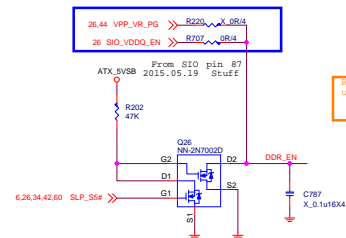
VID	Reference Voltage (V)
H	0.675
L	0.75

Irms = Iout \* SQRT(D/N - (D)^2)  
VCCDDR:  
D=Vout/Vin=1.2/5=0.24  
N=Phase number=1  
=26.2A\*SQRT(0.24-0.0576)  
=11.2A

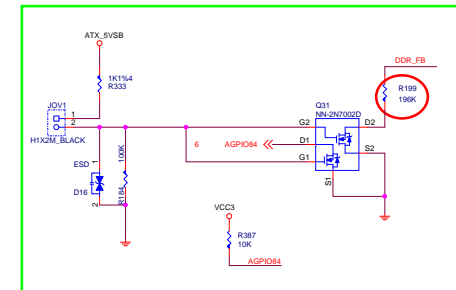


6.42,46,47,48 APU\_AMARI >> D11 >> S4LR8020S-40T1G-HF VPP\_VR\_PG

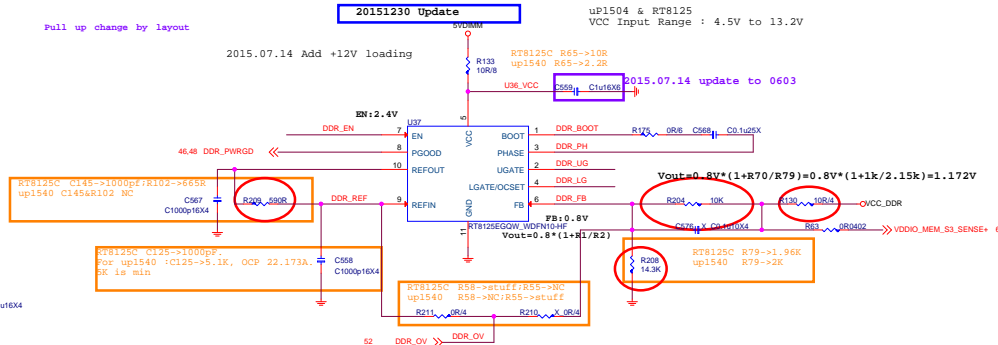
Pull up change by layout



6.26,34,42,60 SLP\_S58 >> G2 >> D1 >> S2 >> C787 X.0.1uF6X4



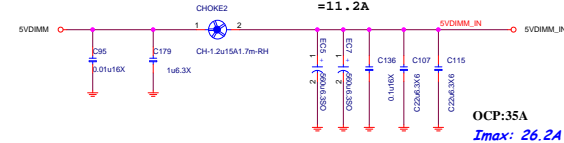
2015.07.14 Add +12V loading



OCP=35A  
OCPreftrain 5Kohm  
OCP  
=(R232\*10uA)/Rdsom  
=R232\*10uA/3.3m/2  
=35A  
R232=5.775k

#### UPI VOLTAGE CONSOLE

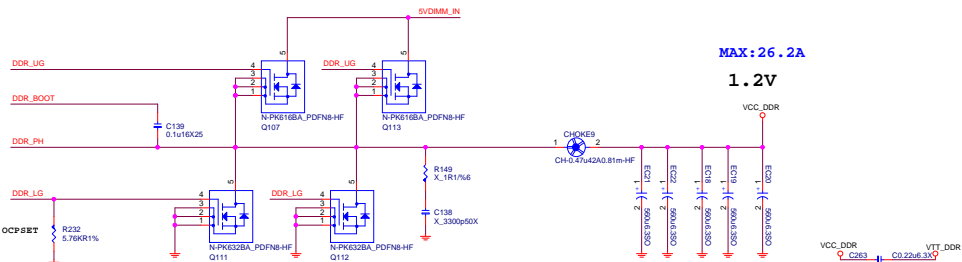
0x26:RH=18K,RL=13K



OCP:35A  
Imax: 26.2A

MAX:26.2A

1.2V



MICRO-STAR INT'L CO.,LTD

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10	DDR Power-RT8125E		10
45			45

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FOR CPU 1.8V S5

0.5A

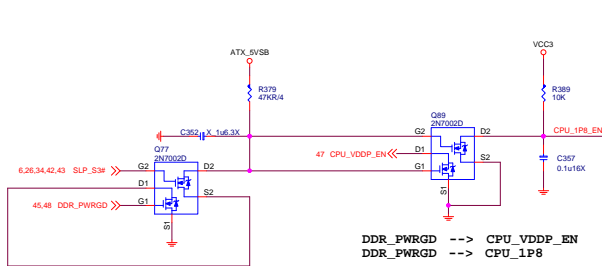
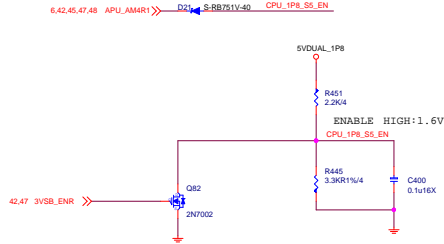
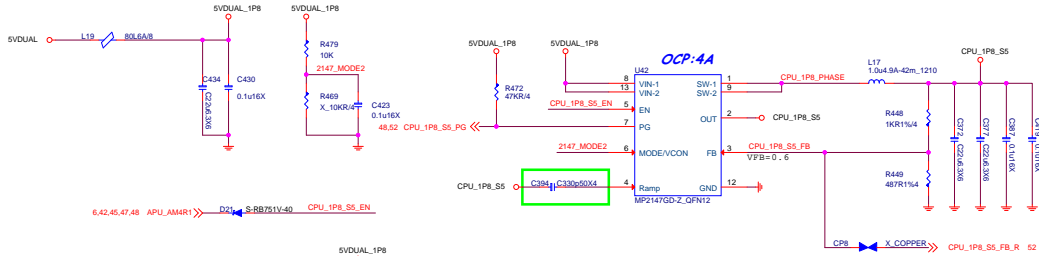
FOR VCCP\_SOC\_S5

0.9A

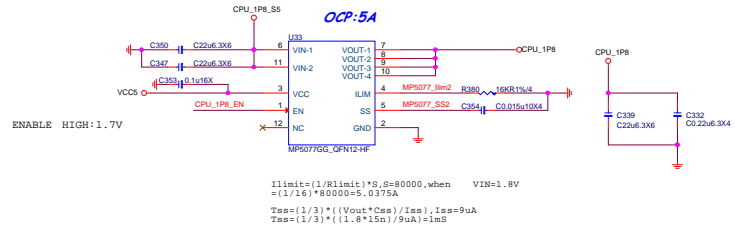
FOR CPU 1.8V S0

2.0A

$0.5A + 2.0A + 0.9A = 3.4A$

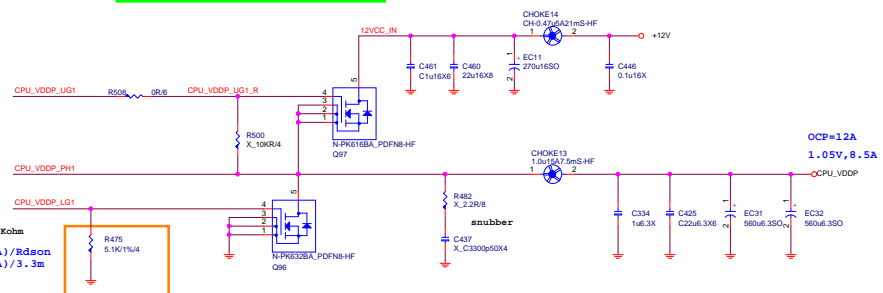
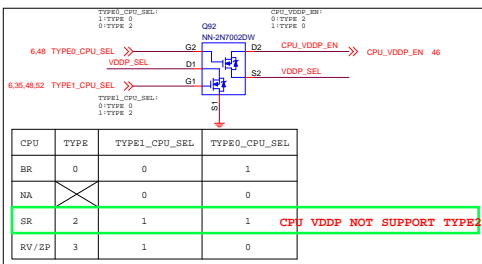
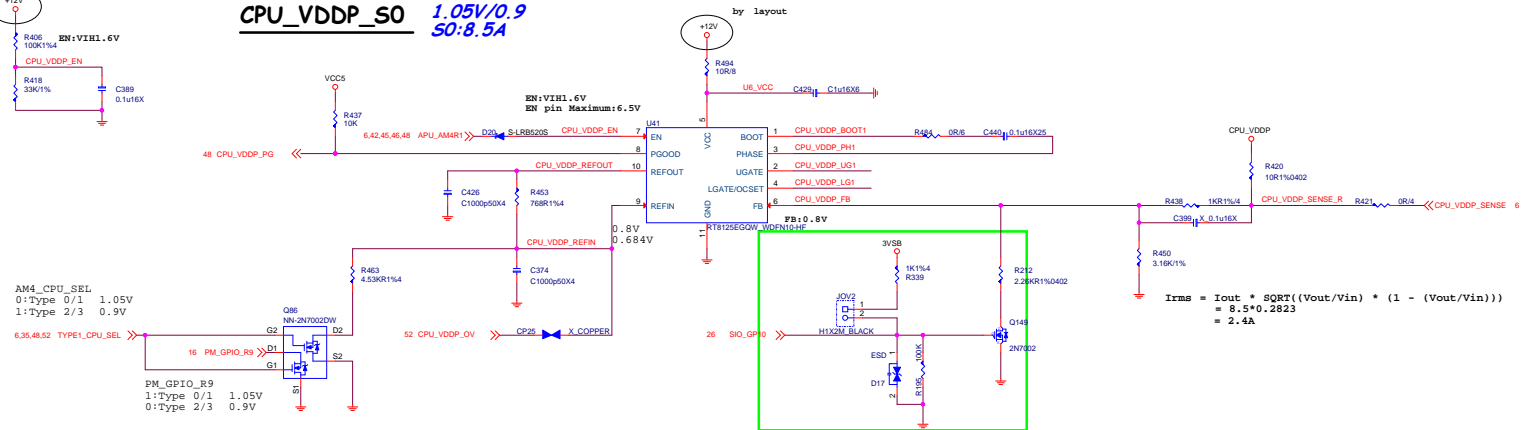


DDR\_PWRGD --> CPU\_VDDP\_EN  
DDR\_PWRGD --> CPU\_1P8

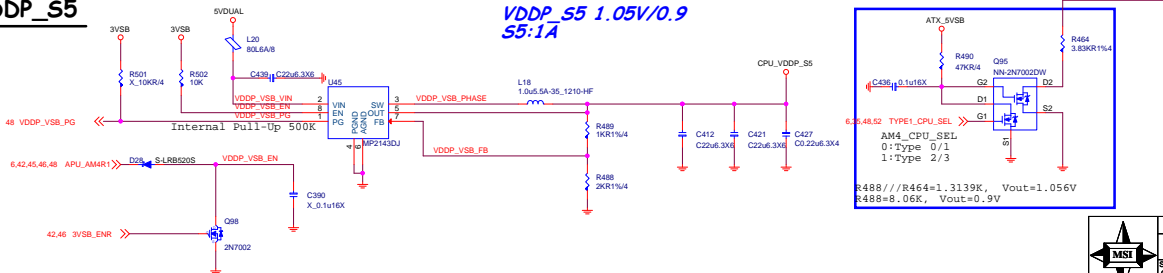


$I_{limit} = (1/R_{limit}) * S, S = 80000, \text{when } VIN = 1.8V$   
 $= (1/16) * 80000 = 5.0375A$   
 $T_{ss} = (1/3) * ((V_{out} * C_{ss}) / I_{ss}), I_{ss} = 9uA$   
 $T_{ss} = (1/3) * ((1.8 * 15n) / 9uA) = 1mS$

CPU\_VDDP\_S0      1.05V/0.9  
S0:8.5A



## CPU\_VDDP\_S5



**MICRO-STAR INT'L CO.,LTD**

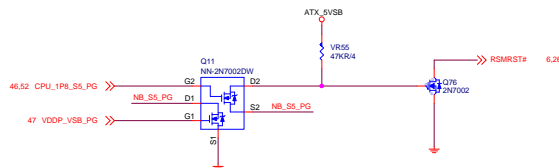
MS-7A32


Size	Document Description
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Custom	CPU Power VDDP-R1812SE	10
Date: Thursday, February 23, 2017	Sheet	47 of 65

[illegible][illegible]

S0	PG
<hr/>	
S5	PG

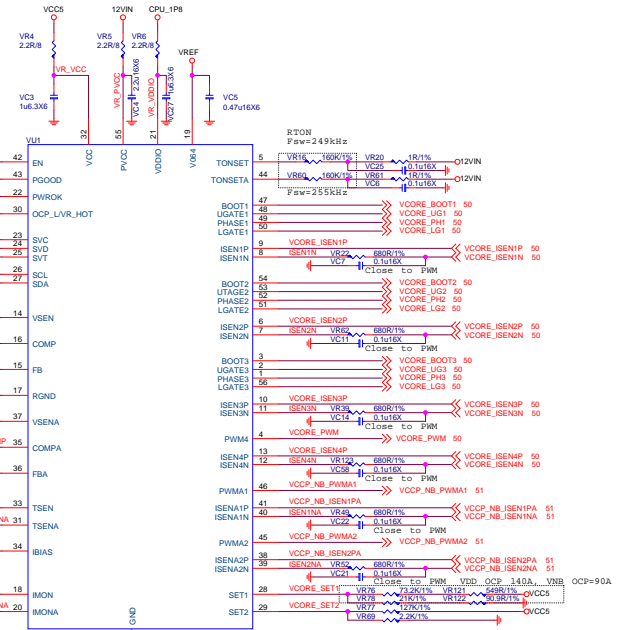
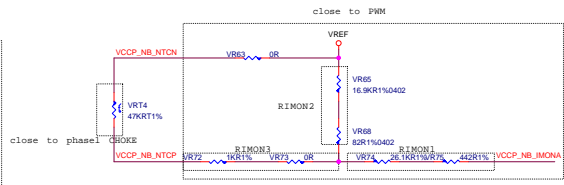
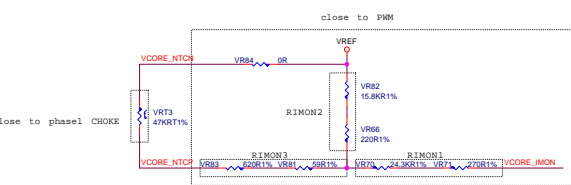
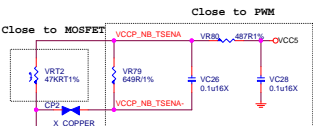
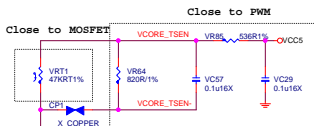
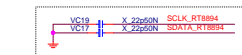
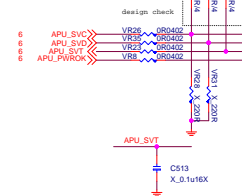


CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/VP	3	1	0

CPU VDDP NOT SUPPORT TYPE:

When you use external buffer  
then you cannot let APU PWR\_GOOD pin float  
in any sleep state.  
If you're buffer use 3.3V\_S0 and you need Pull-down 100K  
If you're buffer use 3.3V\_S5 and you don't need PD.



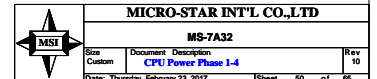


```
SET1 control ICCMAX,OCP setting
SET2 control Internal compensation
```

```
VCORE IccMAX: 125A ==>OCP==>140A
VCC NB IccMAX: 75A ==>OCP==> 95A
```

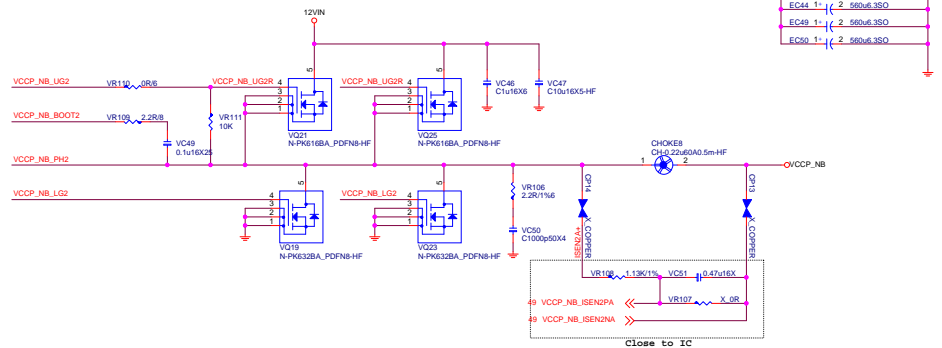
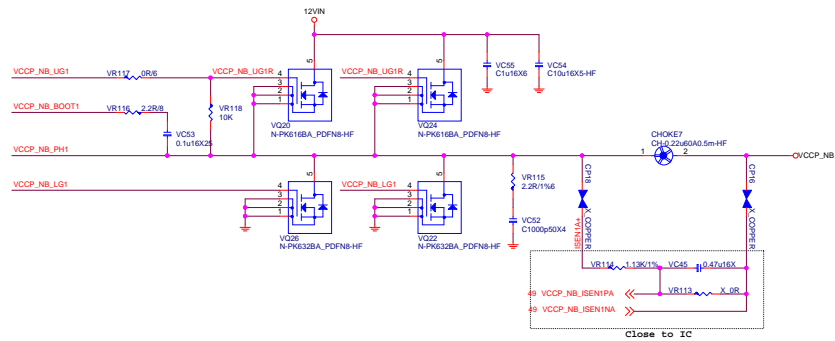
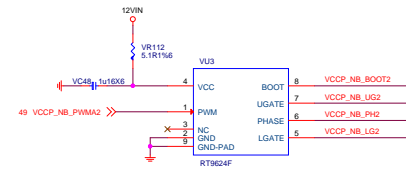
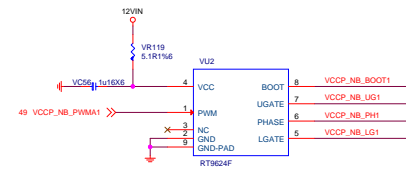


0.75V~1.5V



VCCP\_NB 95W TDC:50A EDC:75A  
VCCP\_NB 65W TDC:50A EDC:75A

0.75V~1.2V

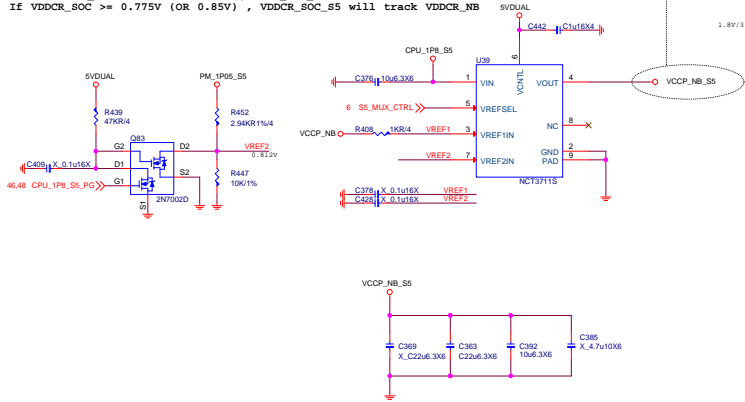


FOR VCCP\_SOC\_S5  
0.9A

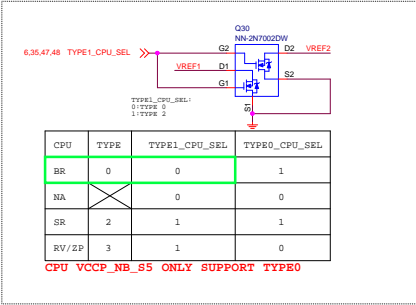
TYPE0 Only

S5\_MUX\_CTRL  
HIGH:S0  
LOW: S3/S5

H: +VDDCR\_FCH\_ALW will track VDDNB  
L: If VDDCR\_SOC<0.775V (OR 0.85V), VDDCR\_SOC\_S5 =0.775V.  
If VDDCR\_SOC >= 0.775V (OR 0.85V) , VDDCR\_SOC\_S5 will track VDDCR\_NB



(VDDCR\_SOC\_S5 is only used for AMD Family 15h Models 60h-6Fh processors) Bristol Ridge TYPE0

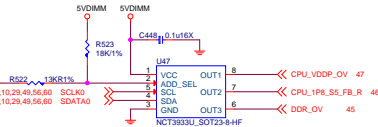


CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP\_NB\_S5 ONLY SUPPORT TYPE0

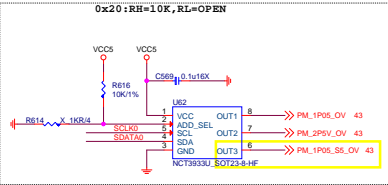
Over Voltage Control IC

0x26:RH=18K,RL=13K

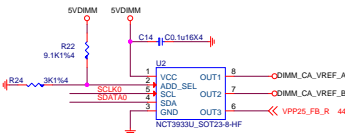


除時間調整外,能有任何幫助,否則不上N CT3933與相關器項

0x20:RH=10K,RL=OPEN



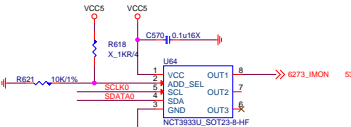
0x28:RH=9.1K,RL=3K



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (Kohm)	OPEN	3.9	3	2.2	1.3	10
RL (Kohm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

0x2A:RH=OPEN,RL=10K



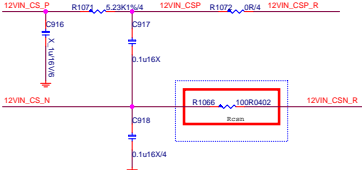
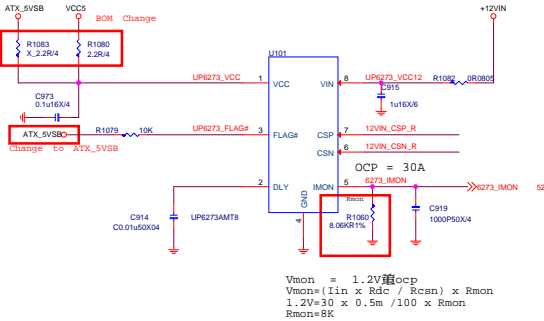
MICRO-STAR INT'L CO.,LTD

MS-7A32

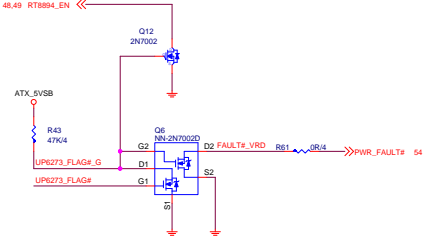
Star Custom Document Description CPU Power NB Switch/NCT3933 Date: Thursday, February 23, 2017 Issued 62 of 65

uP6273 CURRENT SENSE

VCORE EDC MAC 125A  
NB EDC MAX75A



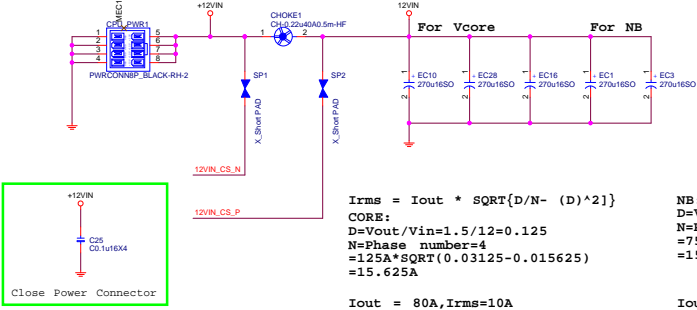
$I_{mon} = 10\mu A = V_{in} / 2A$  (NCT3933)  
 $I_{in} \times R_{dc} / R_{can} = I_{mon}$   
 $2A \times 0.5m / R_{can} = 10\mu A$   
 $R_{can} = 100\text{ ohm}$



CPU POWER CONNECTOR

uP6273 CURRENT SENSE

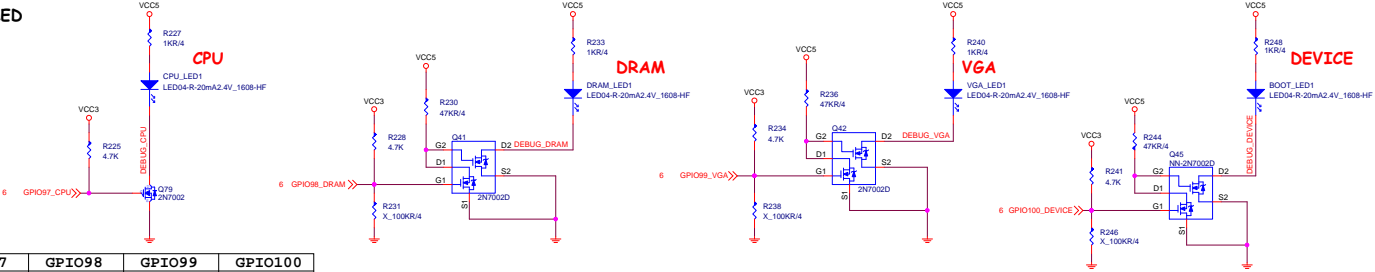
VCORE EDC MAC 125A  
NB EDC MAX75A



$I_{rms} = I_{out} \times \sqrt{D/N - (D)^2}$   
NB:  
 $D = V_{out} / V_{in} = 1.2 / 12 = 0.125$   
 $N = \text{Phase number} = 2$   
 $= 75A \times \sqrt{0.05 - 0.01}$   
 $= 15A$   
 $I_{out} = 80A, I_{rms} = 10A$   
 $I_{out} = 50A, I_{rms} = 10A$

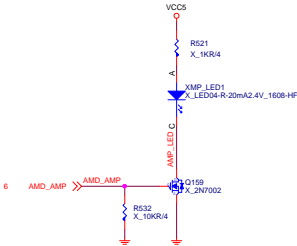


EZ Debug LED

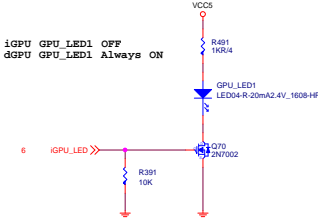


LED	GPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮		GPI FULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅		GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

AMD AMP Detect LED



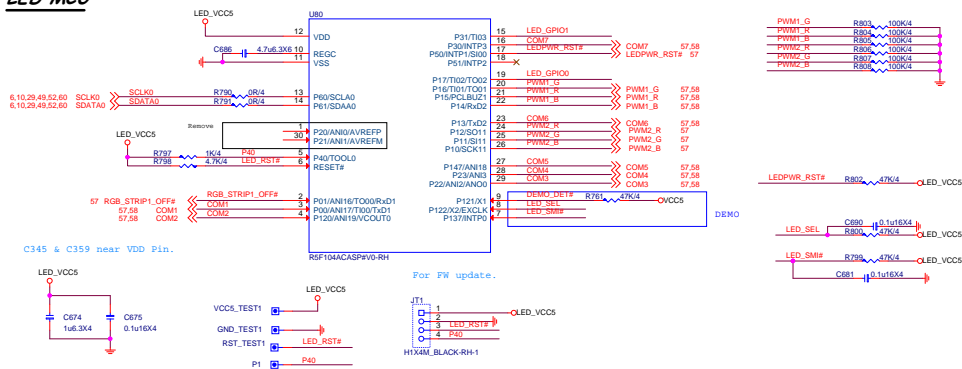
AM4 APU Detect LED Circuit



LED	x16	x8	x4
PCIE2	Red	White	White

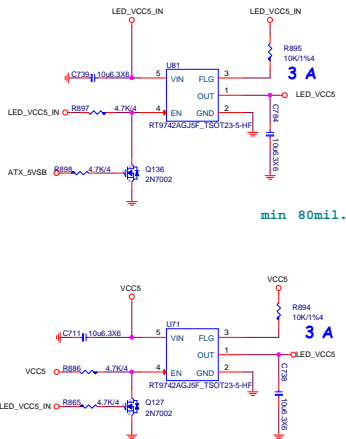
GPIO	EGPIO95	EGPIO96
亮	GPO PO HIGH	GPO PO HIGH
滅	GPI (default LOW)	GPI (default LOW)

## LED MCU

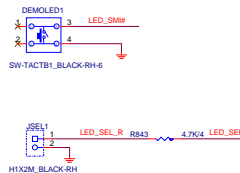


Control	Net Name	PWM USE	Connector
PCH	LED_GPIO1	No Use	JPIPE_LED2
Audio	COM1-7	PWM1	RGB_LED
Board Side LED	COM1-7	PWM2	RGB_LED
LED STRIPLINK	RGB_STRIP1_OFF#	PWM1	JLED1
IO Cover	LED_GPIO0	No Use	JPIPE_LED1

## EXTERNAL POWER INPUT

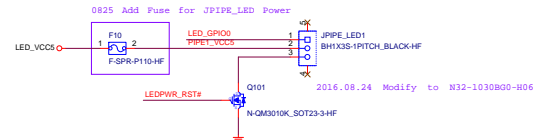


## LED Demo Button



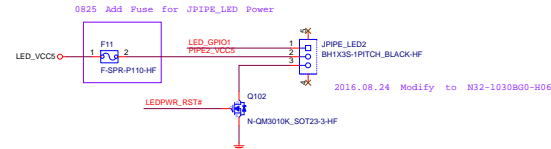
## Cover LED

6PCS LED\*0.16W=0.96W



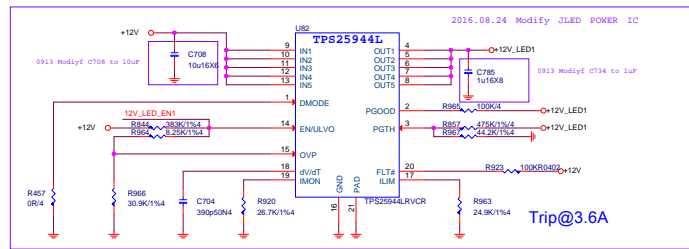
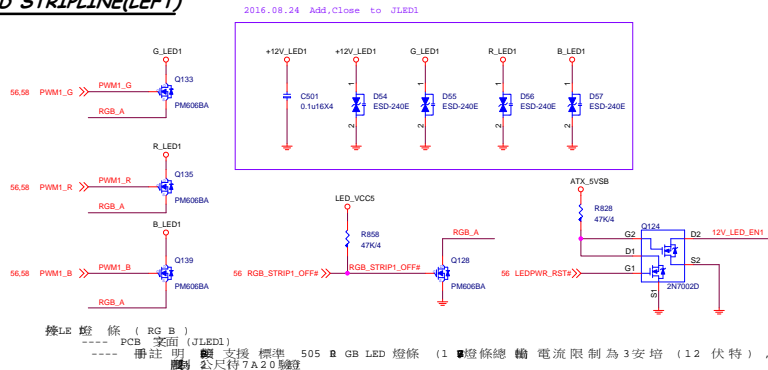
## HEATSINK LED

9PCS LED\*0.16W=1.44W

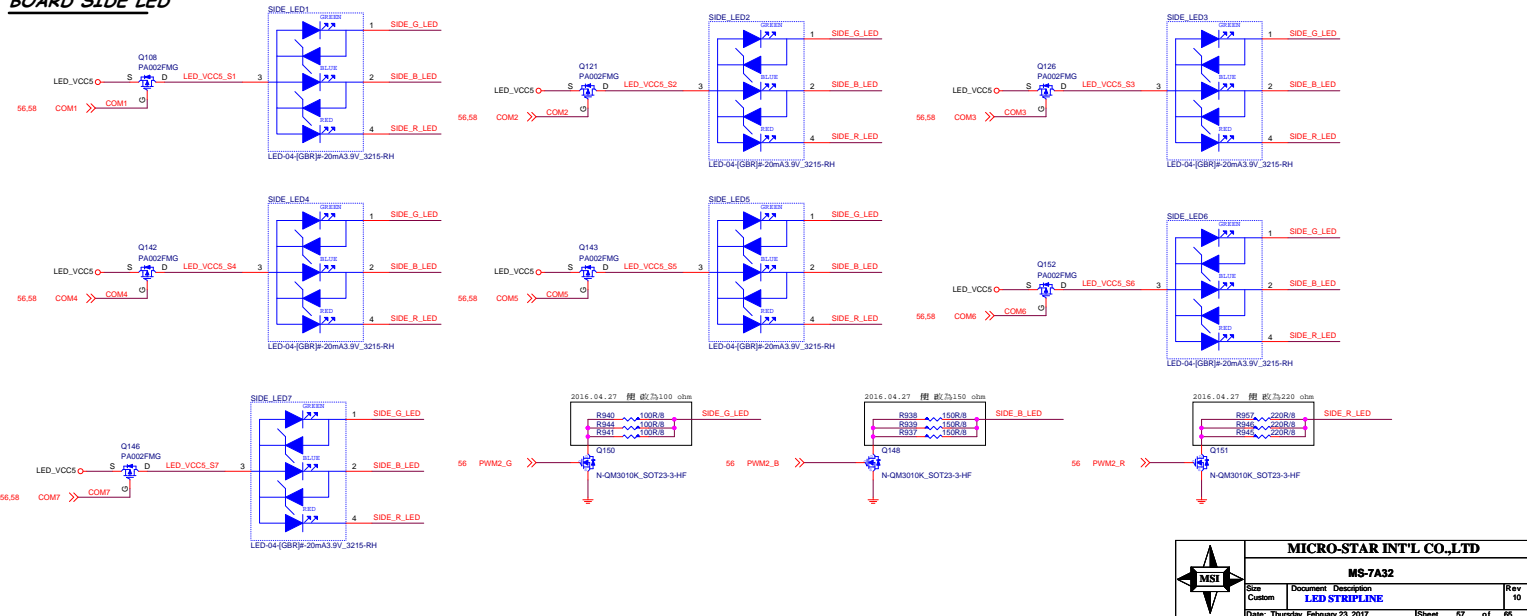




## LED STRIPLINE(LEFT)

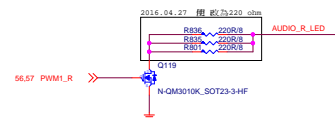
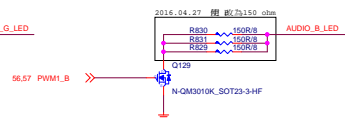
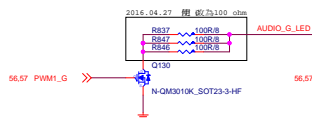
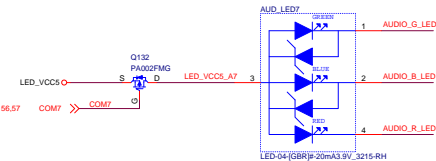
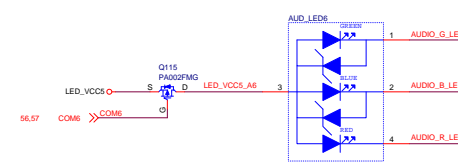
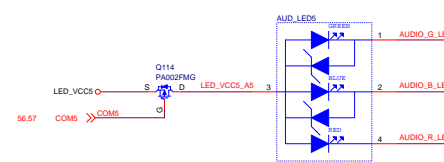
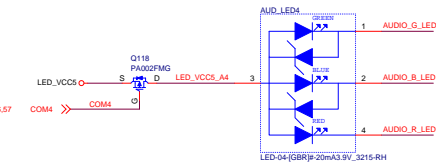
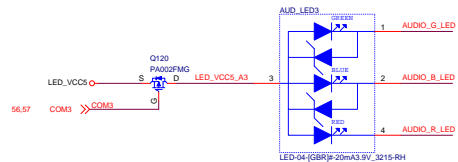
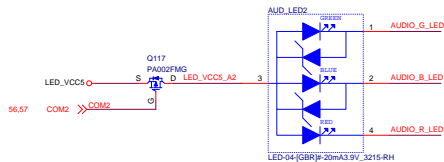
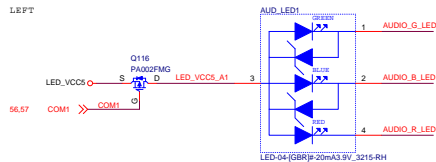


## BOARD SIDE LED



# AUDIO\_MOAT\_LED

LEFT



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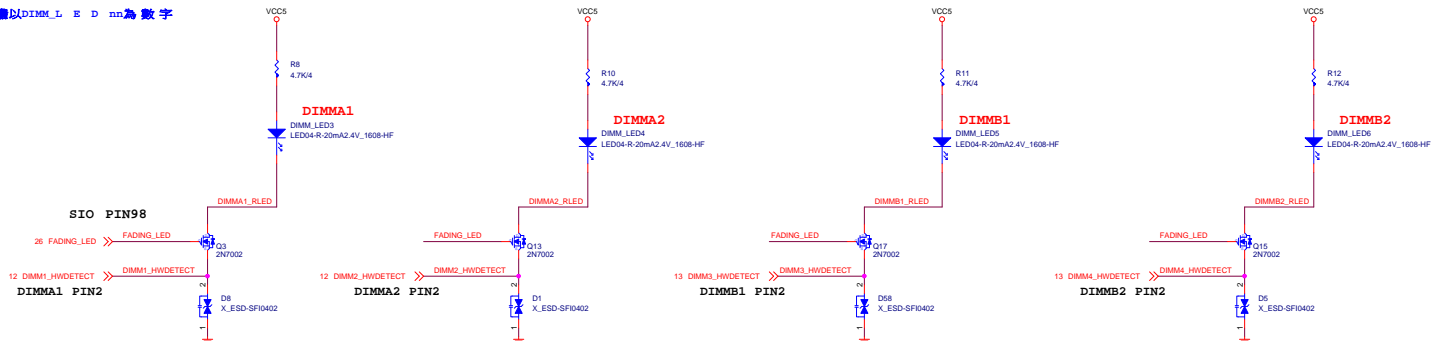
MS-7A32

Rev	Description	Docu	Star
10	LED AUDIO	Custom	Star
61	68	58	16

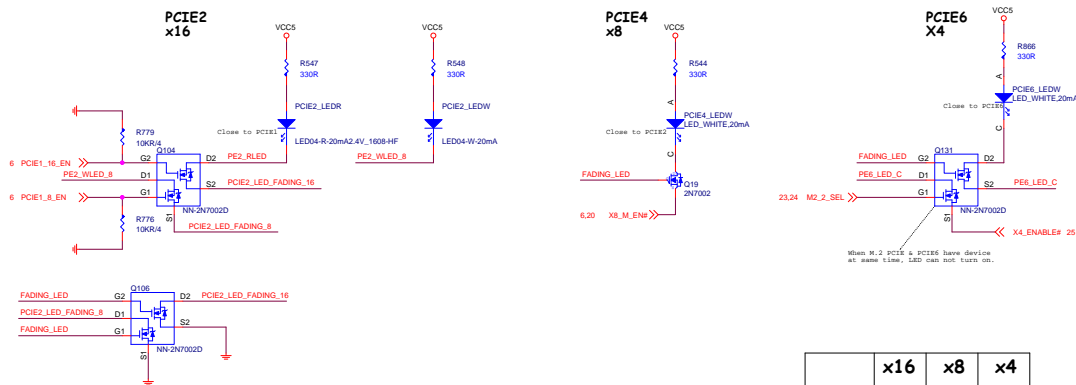
Date: Thursday, February 23, 2017

紅： D0C-040S500-R07

LED 繼以DIMM\_L E D nn為數字



**PCIE SLOT LED**



	x16	x8	x4
PCIE1	Red	X	X
PCIE4	X	White	X
PCIE6	X	X	White



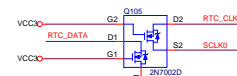
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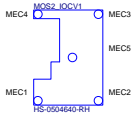
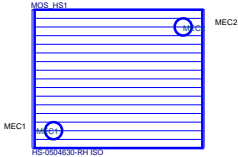
Size Custom	Document Description <b>LED DIMM/PCIE</b>	Rev 10
Date: Thursday, February 23, 2017		Sheet 59 of 65



## 2017/2/22 Modify for G3 CLR\_CMOS



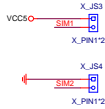
HEAT SINK



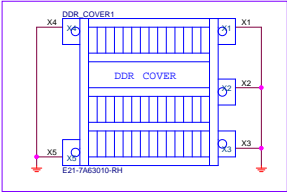
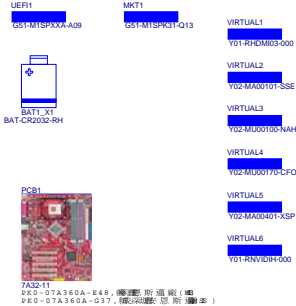
CPU Socket



Simulation



MANUAL PART

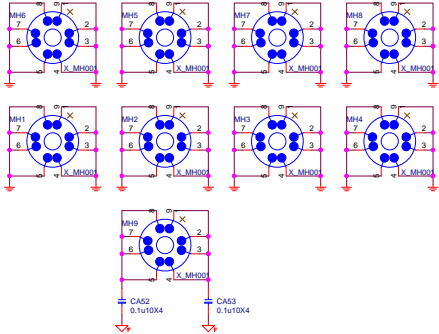


0901 Modify DDR\_COVER1 PIN X1.X2.X3.X4.X5 Connect to GND

VR Cover

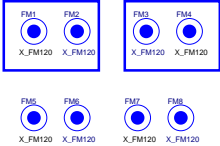


Optics Orientation Holes




5010

5020



OPT	Configure	BOM	Function
		601-7A32-010	XXXX



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MS-7A32

Star Custom

Document Description  
BOM Option

Date: Friday, February 28, 2017

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